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Current-steering transimpedance amplifiers for high-resolution digital-to-analogue converters

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Abstract- A family of current-steering transimpedance amplifier circuits is presented for use in high-resolution, digital-to-analogue converters. The problems of achieving accurate current-to-voltage conversion are discussed with a specific emphasis on digital audio applications. Comparisons are made with conventional virtual-earth feedback amplifiers and the inherent distortion mechanisms relating to dynamic open-loop gain are discussed. Motivation for this work follows the introduction of DVD-audio carrying linear PCM with a resolution of 24 bit at a sampling rate of 192 kHz.

1   Introduction

This paper investigates the design and performance requirements of the transimpedance amplifier used in association with a current-output, digital-to-analogue converter (DAC) [1]. The principal motivation for this work stems from the extreme resolution requirements determined by the advanced audio specification available in digital versatile disc (DVD) applications [2]. Following a theoretical discussion, two principal circuit topologies are presented, the first based upon wide-band, current steering circuit techniques enhanced by input-stage error correction [3], while the second incorporates dual operational amplifiers with nested differential feedback and an embedded low-pass filter.

The DVD-video specification includes linear pulse-code modulation (LPCM) at 96 kHz sampling with a 24-bit resolution while DVD-audio extends this to a maximum of 192 kHz at 24 bit in its two-channel mode. Although DVD includes alternative audio formats such Dolby AC-3[1] and DTS[2] together with lower specification LPCM options, it is the most demanding parameters that dictate the performance requirements of the converters and associated analogue circuitry. Techniques incorporating oversampling and multi-bit noise shaping DACs have been proposed to achieve the required accuracy, which include methods to randomise DAC errors to decorrelate distortion into a noise residue [4,5]. The performance of R-2R ladder network DACs has also improved where accuracy exceeding 21 bit is now claimed for consumer grade products.

However, although the performance of the digital processing and digital converter circuitry can be exemplary, there are error mechanisms in the analogue circuitry immediately following the DAC which produce non-linear distortion. Most multi-bit DACs are current-output devices and should therefore drive low (ideally zero) input impedance transimpedance amplifiers to perform current-to-voltage conversion (I/V conversion). However, DACs operate at high sampling frequencies, typically ≈ 384 kHz, and produce rapid changes in output current with typically nano-second settling times. Consequently, a transimpedance amplifier requires a rapid yet linear response time with low dynamic modulation of its principal parameters.

Distortion mechanisms are discussed specific to a transimpedance amplifier driven by a rapidly changing input current. The errors are assessed both by linear and non-linear analysis including simulation, where it is shown that differential-phase distortion induced by non-linearity, can be represented approximately as an additional correlated jitter distortion [6]. Solutions to these problems are presented that employ fast acting, current steering circuitry augmented by novel input-stage error correction to both linearize and lower the input impedance, also a 2-stage amplifier is investigated.

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[1] Dolby AC-3: proprietary multi-channel, lossy perceptual coding algorithm.
[2] Digital Theatre Systems (trade name): proprietary multi-channel, lossy perceptual coding algorithm.

2 Virtual-earth transimpedance amplifier and transient distortion mechanisms

Distortion mechanisms in transimpedance amplifiers can be attributed jointly both to linear and to non-linear aspects of circuit behaviour. In the following Section some global observations are made and critical circuit factors examined.

2-1 Linear distortion in I/V conversion

A common approach to transimpedance amplifier design is to use a single high-gain, wide-bandwidth operational amplifier as illustrated in Figure 2-1.
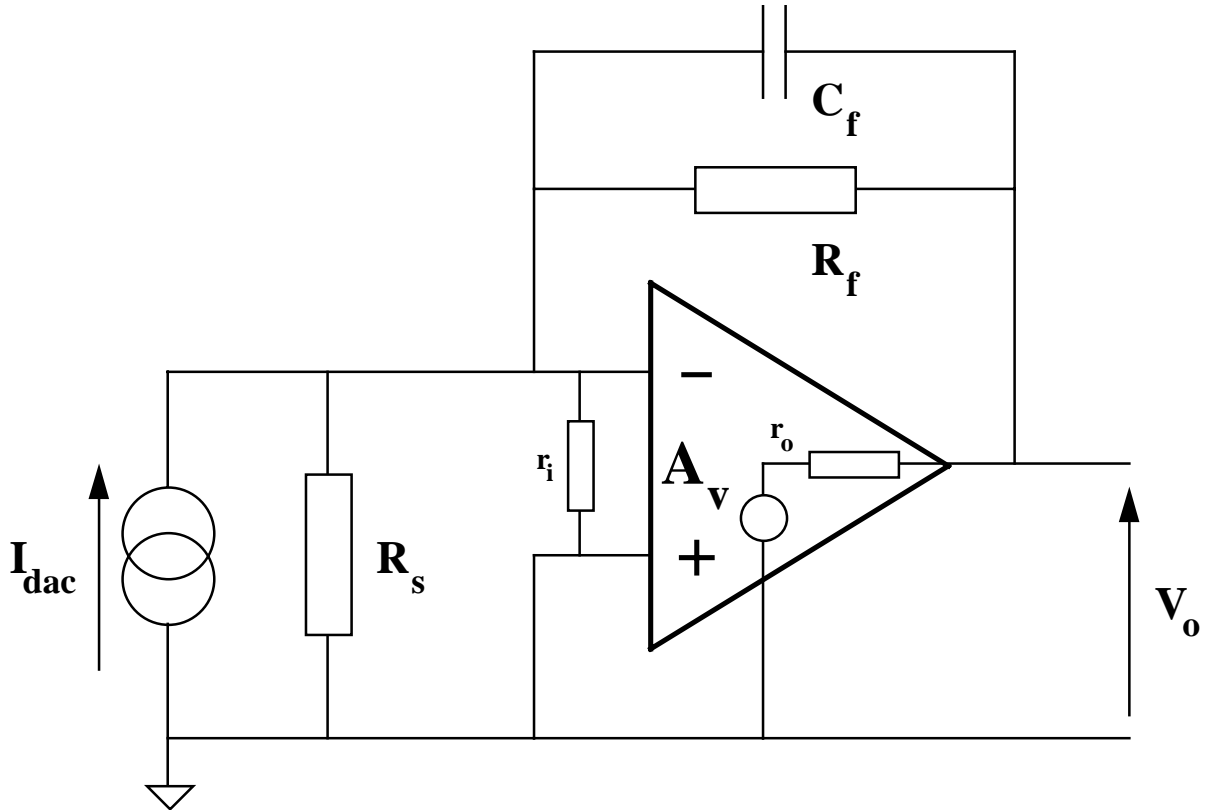

Figure 2-1 Transimpedance amplifier using operational amplifier with feedback.

The DAC output is represented as a Norton equivalent circuit with current generator I_{dac} and source resistance R_s. The operational amplifier is configured in shunt feedback mode with feedback impedance Z_f formed here by resistor R_f in parallel with capacitor C_f. This circuit yields a low value of input impedance z_{in} given by,

$$z_{in} = \left(\frac{R_f}{1 + j2\pi f R_f C_f} \right)\left(\frac{1}{1 + A_v} \right) \;//\; r_i = \frac{Z_f \,//\, r_i}{1 + A_v}$$

For the operational amplifier, A_v is the differential voltage gain and r_i is the differential input impedance that normally can be neglected, reducing z_{in} to,

$$z_{in} \approx \frac{Z_f}{1 + A_v} \qquad\qquad\qquad \text{… 2-1}$$

For the case where $z_{in} \ll R_s$, then the current I_{dac} flows predominantly through the feedback impedance and for the ideal case of a vanishingly small differential input voltage, the target transimpedance $Z_T(f)$ is

$$Z_T(f) \quad = \quad \frac{V_o}{I_{dac}} \quad = \quad -Z_f \qquad \qquad \text{... 2-2}$$

Equation 2-2 describes perfect I/V conversion and assumes $A_v = \infty$ for all frequency. However, in practical circuits even a good approximation to this criterion is difficult to achieve because of the wide bandwidth of the current signal I_{dac} that results from the rapid changes at sample boundaries. This aspect of performance will be examined in the paper and shown to be of particular significance.

Consider a transimpedance amplifier using an operational amplifier with an n-pole transfer function, where the differential voltage transfer function A_v is given by,

$$A_v \quad = \quad \frac{A_{v0}}{\sum_{r=0}^{r=n-1}\left(1 \; + \; j\frac{f}{f_r}\right)} \qquad \qquad \text{... 2-3}$$

where f_0, to f_{n-1} are n respective break frequencies and A_{v0} is the zero-frequency differential voltage gain. If z_{in} is the effective input impedance of the transimpedance amplifier then the differential input voltage v_ε at the virtual earth is,

$$v_\varepsilon \quad = \quad I_{dac}\frac{z_{in}R_s}{z_{in} \; + \; R_s}$$

where by including $Z_T(f)$ from equation 2-2, the output voltage V_o is,

$$V_o \quad = \quad -Z_f\left(I_{dac} \; - \; \frac{v_\varepsilon}{r_i}\right) \; - \; v_\varepsilon \quad = \quad Z_T(f)I_{dac} \; - \; v_\varepsilon\left(1 + \frac{Z_T(f)}{r_i}\right)$$

In practice the input current to the operational amplifier is negligible as v_ε is small and r_i is large, so can be neglected. Consequently, eliminating v_ε the transimpedance $Z_A(f)$ is,

$$Z_A(f) \quad = \quad \frac{V_o}{I_{dac}} \quad = \quad Z_T(f) \; + \; \frac{z_{in}R_s}{z_{in} \; + \; R_s} \quad \approx \quad Z_T(f) \; + \; z_{in} \qquad \qquad \text{... 2-4}$$

To quantify the error in the transimpedance response, an error function E(f) is defined as,

$$E(f) \quad = \quad 1 \; - \; \frac{Z_A(f)}{Z_T(f)} \qquad \qquad \text{... 2-5}$$

Substituting for $Z_A(f)$ from equation 2-4, and incorporating equations 2-1, 2-2 and 2-3,

$$E(f) \quad = \quad -\frac{z_{in}}{Z_T(f)} \quad = \quad \frac{1}{1 + A_v} \quad = \quad \frac{\frac{1}{A_{v0}}\sum_{r=0}^{r=n-1}\left(1 \; + \; j\frac{f}{f_r}\right)}{1 + \frac{1}{A_{v0}}\sum_{r=0}^{r=n-1}\left(1 \; + \; j\frac{f}{f_r}\right)} \qquad \qquad \text{... 2-6}$$

Equation 2-6 reveals an error function dependent only on the operational amplifier parameters.

Differential-phase distortion $\Delta\phi$

The differential-phase distortion $\Delta\phi$ is defined as the additional phase shift of the transimpedance amplifier introduced by the finite gain and frequency characteristics of the operational amplifier. By considering two I/V stages with respective transimpedances $Z_T(f)$ and $Z_A(f)$, the difference in phase response, hence $\Delta\phi$ is,

$$\Delta\phi \quad = \quad \arctan\left(\frac{Z_T(f)}{Z_A(f)}\right) \quad = \quad \arctan\left(1 \,-\, E(f)\right) \quad = \quad \arctan\left(\frac{A_v}{1 \,+\, A_v}\right) \qquad \ldots 2\text{-}7a$$

where substituting for A_v from equation 2-3,

$$\Delta\phi \quad = \quad -\arctan\left(1 \,+\, \frac{1}{A_{v0}}\sum_{r=0}^{r=n-1}\left(1 \,+\, j\frac{f}{f_r}\right)\right) \qquad \ldots 2\text{-}7b$$

The differential group delay T_{diff} is then calculated as,

$$T_{diff} \quad = \quad -\frac{1}{2\pi}\frac{\partial\Delta\phi}{\partial f} \qquad \ldots 2\text{-}8$$

2-2   Non-linear distortion in I/V conversion

The analysis presented in Section 2-1 demonstrates a benign linear distortion that is well controlled in the audio band by feedback providing there is adequate closed-loop gain. Also, the high output impedance of the DAC makes the feedback factor almost unity gain and nearly independent of the feedback path components R_f and C_f. However, for transient input currents that occur at sample boundaries, there can be modulation of the open-loop parameters of the operational amplifier. At these time instants the operational amplifier may appear almost "open-loop" and experience momentary dynamic changes in gain-frequency response. In extreme conditions the operational amplifier can exceed its slew-rate limit contributing further to transimpedance non-linearity, which in turn is reflected in the input impedance.

Non-linearity is modelled here for two cases: The first where no slew rate limiting occurs and there is only minor modulation of the operational amplifier gain as a function of its differential input signal and the second, where momentary slew-rate limiting also occurs.
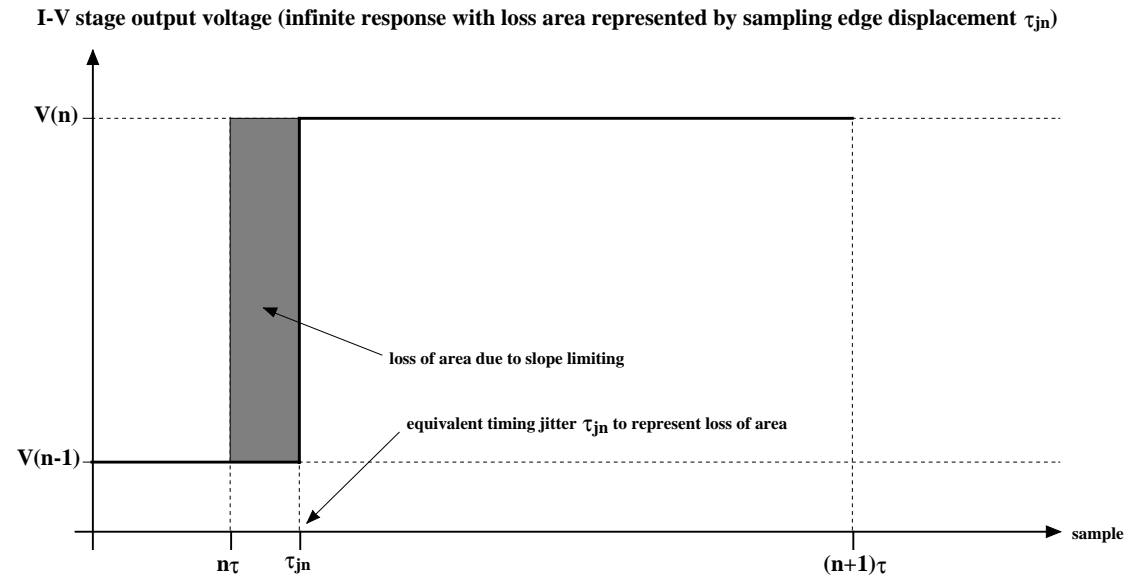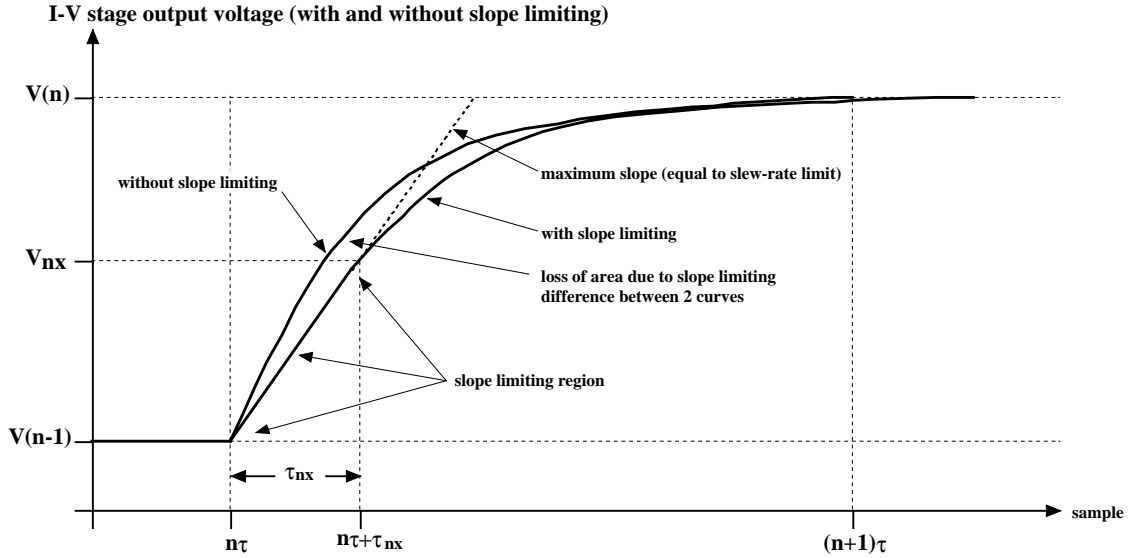
Consider a change in DAC output current from I(n-1) to I(n) at the nth sample where the sampling interval is τ. Assume the operational amplifier has positive and negative slew-rate limits of $\langle S_+, S_-\rangle$ volt/s and that the DAC output current is a step function. Figure 2-2 shows the output voltage waveform of the transimpedance amplifier, where the response may be divided into two regions. The first region is where the rate-of-change of the output voltage exceeds the slew-rate limit and has constant slope while in the second region, the waveform is controlled by the operational amplifier and its associated feedback network and the output approximates to an exponential waveform. The occurrence of slew-rate limiting causes an error in the area under the reconstructed sample compared to that of linear case.

2-2-1   Linear case

The area under reconstructed sample n for the linear case is defined as A_l. At sample n, the initial output voltage of the transimpedance amplifier is V(n-1), while at sample n+1, due to the finite response time of the amplifier, the output voltage attains a value V(n). Assuming an exponential linear response, the instantaneous waveform v(nτ+t), for $0 < t < \tau$, is given by,

$$v(n\tau + t) \quad = \quad V(n) \quad + \quad \left\{V(n-1) \,-\, V(n)\right\}\, e^{-2\pi f_0 t}$$

where the maximum (initial) slope $= 2\pi f_0\{V(n) - V(n-1)\}$.

4

I-V stage output voltage (with and without slope limiting)

I-V stage output voltage (infinite response with loss area represented by sampling edge displacement τ_{jn})

Figure 2-2 Jitter equivalence of slew-induced distortion at a sample boundary.

It is assumed here that the dominant pole in the closed-loop gain produces an exponential waveform between samples with a time constant $\tau_0 = (2\pi f_0)^{-1}$ that is sufficiently small for the exponential transient to have decayed within a sample period τ, that is $e^{-\tau/\tau_0} \ll 1$.

The area A_l under the nth sample is then calculated,

$$A_l \quad = \quad \int_{t=n\tau}^{(n+1)\tau} v(t)dt$$

giving,

$$A_l \quad = \quad V(n)\tau \quad - \quad \left\{V(n) \; - \; V(n-1)\right\}\left(1 \; - \; e^{-\tau/\tau_0}\right)\tau_0 \qquad \qquad \text{…2-9a}$$

which approximates to,

$$A_l \quad \approx \quad V(n)\tau \quad - \quad \left\{V(n) \; - \; V(n-1)\right\}\tau_0 \qquad \qquad \text{…2-9b}$$

5

2-2-2 Mildly non-linear case without slew-rate limiting

Because a single low-frequency pole normally dominates the operational amplifier response, then within the linear operating region the differential input signal of the amplifier is proportional approximately to the time differential of the input signal. If the operational amplifier exhibits mild non-linearity, then there will be waveform distortion that relates to the inter-sample difference signal. It is therefore proposed to model the non-linearity by modulating the time constant τ_0 by a function of the inter-sample difference signal. That is,

$$\tau_0 \;\Rightarrow\; \tau_{0n} \;=\; \left(1 + \gamma_n\right)\tau_0$$

where,

$$\gamma_n \;=\; \sum_{r=1}^{k} \lambda_r \left(\frac{\left(V(n) - V(n-1)\right)}{V_{max} - V_{min}}\right)^r$$

$\{\lambda_r\}$ are coefficients defining the non-linearity and equation 2-9b is re-written,

$$A_l \;\approx\; V(n)\tau \;-\; \left(V(n) - V(n-1)\right)\tau_{0n} \qquad\qquad \text{...2-10}$$

2-2-3 Non-linear case with slew-rate limiting

In the non-linear case, assume the period τ is divided into two segments, τ_{nx} a period dominated by slew-rate limiting and $\tau - \tau_{nx}$ a linear period with an exponential response with the same time constant as the linear case (although mild non-linearity is introduced later, as in Section 2-2-2). The boundary between the two segments at a level V_{nx} is defined where the initial slope of the exponential at $t = \tau_{nx}$ equals either the positive or negative slew-rate limits of S_+ volt/s or S_- volt/s respectively. If the initial slope, as determined in the linear analysis, of the reconstructed signal case breaches either of these limits then slew-rate limiting occurs, i.e.

$$V(n) - V(n-1) \;>\; S_+\tau_0$$

or

$$V(n) - V(n-1) \;<\; S_-\tau_0$$

In the following analysis, the notation $\langle S_+, S_- \rangle$ implies the slew-rate limit is selected to match the appropriate positive or a negative signal encounter.

In the linear region $\tau > t > \tau_{nx}$,

$$v(n\tau + t) \;=\; V(n) \;+\; \left\{V_{nx} - V(n)\right\} e^{-(t-\tau_{nx})/\tau_0}$$

At the non-linear/linear transition where $v(n\tau + \tau_{nx}) = V_{nx}$ set $\langle S_+, S_- \rangle = \partial v(n\tau + t)/\partial t$, whereby

$$V_{nx} \;=\; V(n) \;-\; \langle S_+, S_- \rangle \tau_0$$

At the termination of the slew-rate-limited region, V_{nx} is,

$$V_{nx} \;=\; V(n-1) \;+\; \langle S_+, S_- \rangle \tau_{nx} \qquad\qquad \text{...2-11}$$

Eliminating V_{nx}, then if the slew-rate limit is exceeded,

$$\tau_{nx} \;=\; \frac{V(n) - V(n-1)}{\langle S_+, S_- \rangle} \;-\; \tau_0 \qquad\qquad \text{...2-12}$$

otherwise,

$$\tau_{nx} = 0 \text{ and } V_{nx} = V(n-1) \qquad \qquad \text{...2-13}$$

By integration, the area A_{ln} under the reconstructed sample for the non-linear case is,

$$A_{\text{ln}} = V(n)\tau - 0.5\{2V(n) - V(n-1) - V_{nx}\}\tau_{nx} - \{V(n) - V_{nx}\}\tau_0 \qquad \text{...2-14}$$

Following the earlier analysis, modify the time constant $\tau_0 \Rightarrow \tau_{0n} = (1 + \gamma_n)\tau_0$ to account for mild non-linearity, where in this case

$$\gamma_n = \sum_{r=1}^{k} \lambda_r \left(\frac{(V(n) - V_{nx})}{V_{max} - V_{min}} \right)^r$$

Hence, the pulse-area error ΔA_{ln} is calculated by taking the difference between the linear and non-linear reconstructed samples and follows from equations 2-9b and 2-14 as,

$$\Delta A_{\text{ln}} = A_l - A_{\text{ln}}$$

$$\Delta A_{\text{ln}} = 0.5\{2V(n) - V_{nx} - V(n-1)\}\tau_{nx} + \{V(n-1) - V_{nx}\}\tau_0 + \gamma_n\{V(n) - V_{nx}\}$$
$$\text{...2-15}$$

Since the DAC output impedance is large, the feedback network $R_f//C_f$ does not effect the degree of negative feedback although it does influence the rate-of-change of output voltage, hence onset of slew induced distortion. In a practical amplifier, C_f can be used to marginally band-limit the input signal and lower the output voltage slope, although it does not reduce significantly the differential input voltage of the operational amplifier, hence internal distortion associated with the early stages of amplification.

2-2-4 Equivalent jitter distortion

The above analysis demonstrates pulse-area modulation located close to sample boundaries that results from non-linearity in the transimpedance amplifier during rapid changes of signal. This non-linear change of area can be mapped approximately to an equivalent sample jitter [6] (absolute jitter τ_{jn} being linked with the nth sample) where the reconstructed samples are otherwise linear. If the equivalent jitter τ_{jn} is only a small fraction of a sample period τ and the sampling frequency is high (e.g. 8 times Nyquist sampling rate), then the approximate distortion is an error impulse of area ΔA_{jn} located at the nth sample given by,

$$\Delta A_{jn} = \{V(n) - V(n-1)\}\tau_{jn} \qquad \qquad \text{...2-16}$$

Consequently, the distortion resulting from transimpedance amplifier non-linearity can be represented as a uniformly sampled sequence $\{\Delta A_{jn}\}$ by equating $\Delta A_{jn} = \Delta A_{\text{ln}}$ or alternatively as an equivalent sample timing jitter sequence τ_{jn}.

3 Example results of operational amplifier based transimpedance stages

This Section presents some example results to demonstrate the typical levels of linear and non-linear distortion inherent in transimpedance amplifiers used with fast switching, current-output DACs.
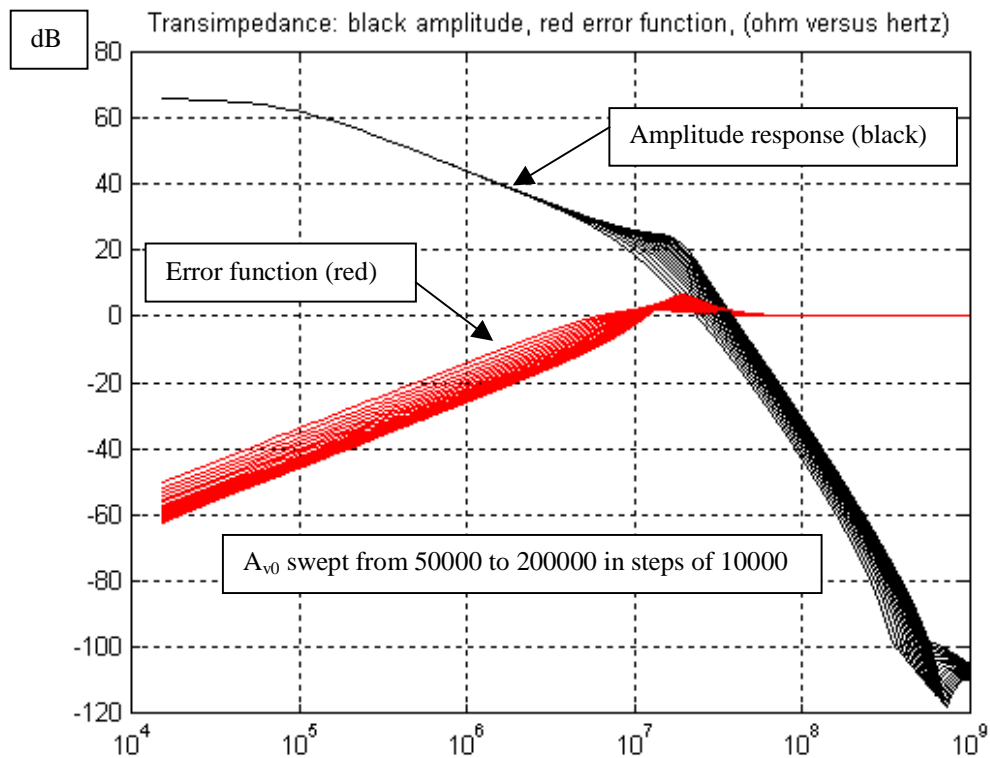
3-1 Linear distortion

By way of example, consider a transimpedance amplifier based on the topology in Figure 2-1, using a 3-pole operational amplifier, where the principal parameters are,
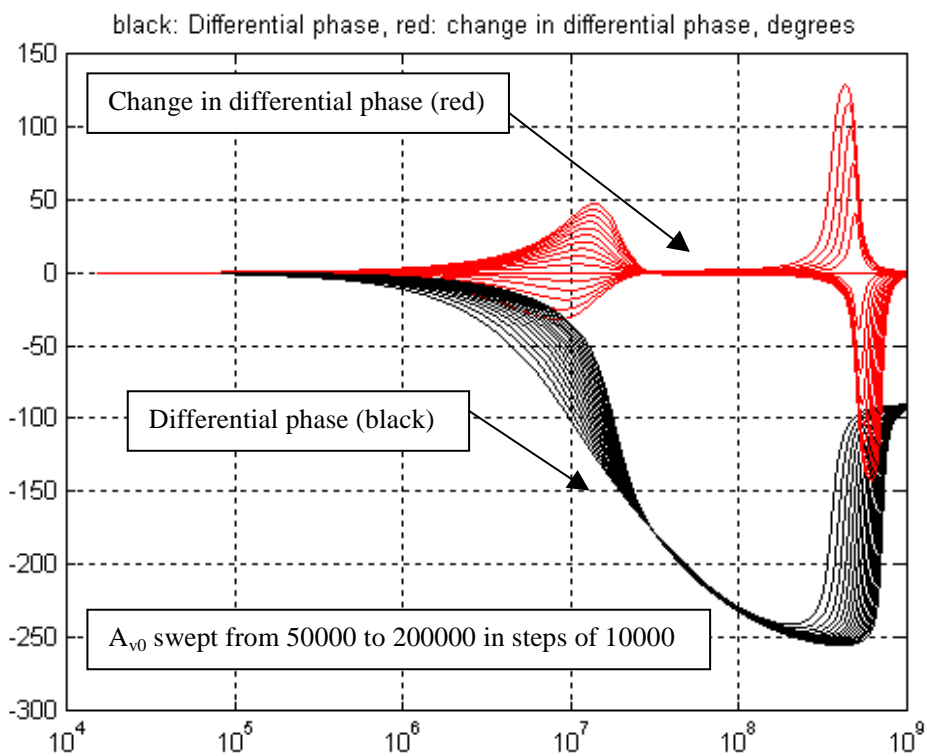
|								
R_s	=	4 kΩ	R_f	=	2 kΩ	C_f	=	1 nF
f_0	=	100 Hz	f_1	=	20 MHz	f_2	=	50 MHz

with dc gain A_{v0} swept from 50000 to 200000 in steps of 10000. The results shown in Figure 3-1 correspond to the transimpedance and error function responses defined in Section 2-1, while those shown in Figure 3-2 and 3-3 correspond to $\Delta\phi$ and T_{diff} respectively as defined by Equations 2-7, 2-8.

Transimpedance: black amplitude, red error function, (ohm versus hertz)

Amplitude response (black)

Error function (red)

A_{v0} swept from 50000 to 200000 in steps of 10000

Figure 3-1 Transimpedance and error function as a function of frequency.

black: Differential phase, red: change in differential phase, degrees

Change in differential phase (red)

Differential phase (black)

A_{v0} swept from 50000 to 200000 in steps of 10000

Figure 3-2 Differential phase error $\Delta\phi$ as a function of frequency for varying A_{v0}.

8
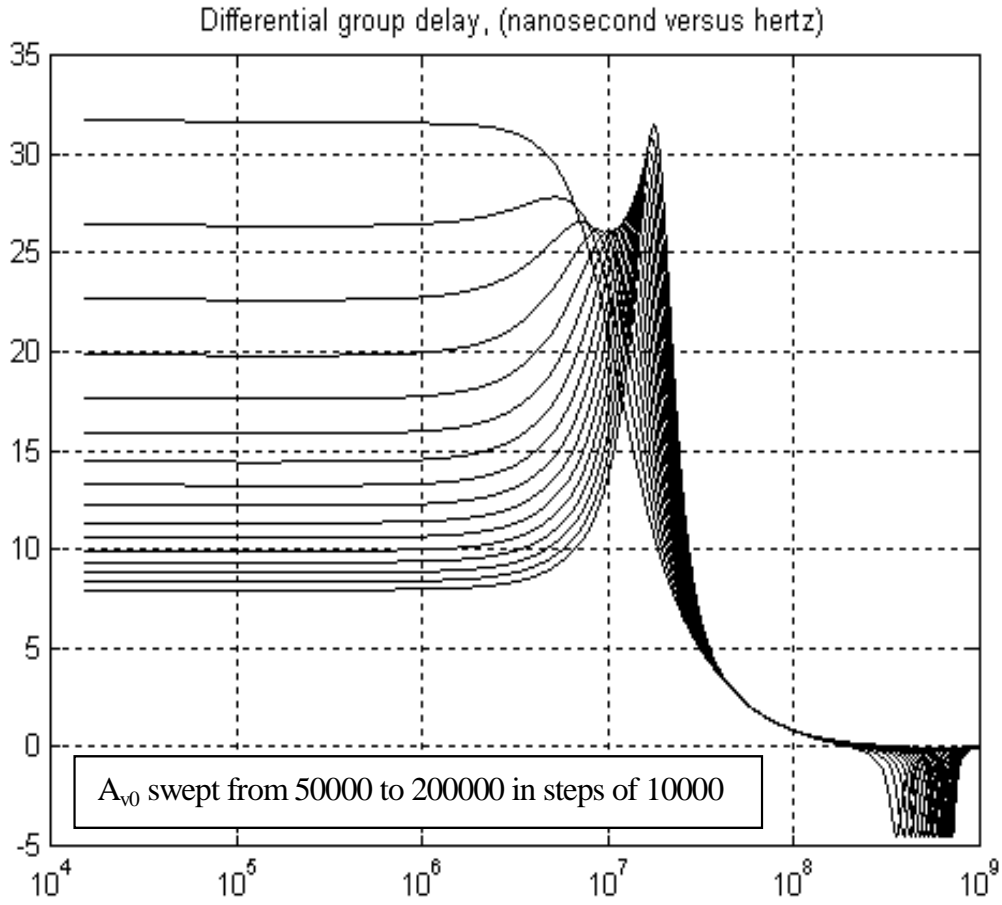
Figure 3-3 Differential group delay T_{diff} as a function of frequency for varying A_{v0}.

Although the analysis presented in Section 2-2-1 is linear, the results illustrate the dependence on A_{v0}, a parameter that may change dynamically both with signal and power supply voltage. Observing $\Delta\phi$ the gross changes appear concentrated at high frequency, yet on closer inspection, T_{diff} reveals that at lower frequency there is an almost constant differential time delay that is strongly dependent on A_{v0}.

To explore this dependency on A_{v0}, a plot of T_{diff} against $(A_{vo})^{-1}$ is presented in Figure 3-4 where the characteristic is almost linear with a slope of $1.5882*10^6$ ns-gain, such that

$$T_{\text{diff}} \quad = \quad \frac{1.5882*10^6}{A_{v0}} \qquad\qquad \ldots \text{3-1}$$

Hence, for a change in dc gain ΔA_{v0}, the corresponding change in group delay ΔT_{diff} is,

$$\Delta T_{\text{diff}} \quad = \quad -\frac{1.5882*10^6}{A_{v0}}\left(\frac{\Delta A_{v0}}{A_{vo}}\right) \qquad \text{nano-second} \qquad \ldots \text{3-2}$$

This implies that for a nominal gain of $A_{v0} = 10^5$, there is a group delay change of 158.82 ps per 1% gain change. It should be noted that because the output resistance of the DAC is significantly greater than the impedance of the feedback network, the values of R_f and C_f are uncritical with respect to the dependence of T_{diff} on A_{v0}.

9
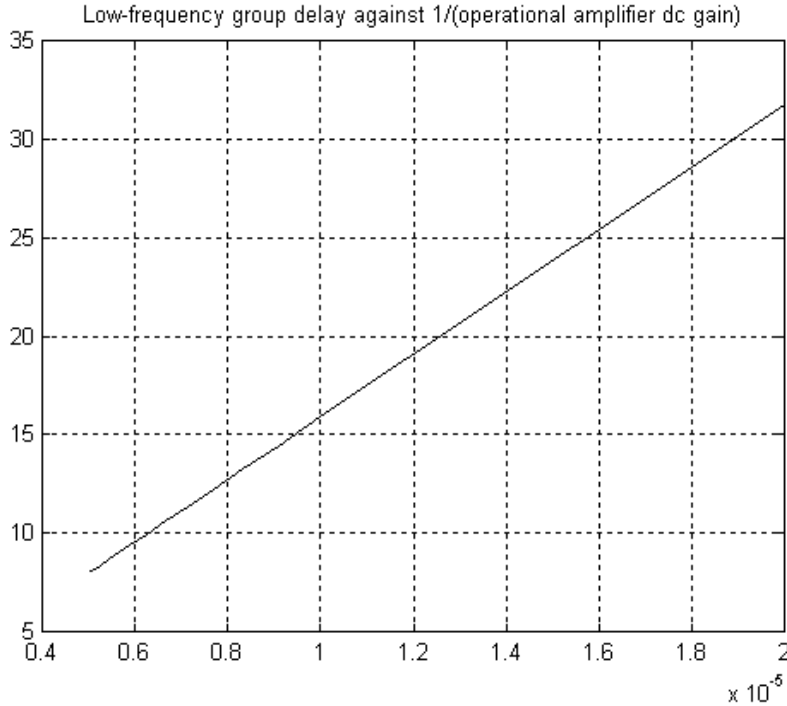
Figure 3-4 Low-frequency differential group delay T_{diff} ns as a function $1/A_{v0}$.

Jitter equivalence

Although these results do not describe non-linear performance in a way that enables exact prediction of distortion, they do give insight into basic mechanisms. For example, the dependency of T_{diff} on A_{v0} can be observed as correlated jitter [6]. Any signal dependent modulation of A_{v0} will cause timing displacement of the signal. This is exacerbated by the presence of high-frequency signal components arising from the structure of sampled audio. In practice there will be modulation of the sampled signal with the dynamic phase-dependent amplifier parameters, allowing high-frequency signal components to alias into the audio band, where examples are presented in Sections 3-2 and 3-3. In making this observation, the role of the feedback capacitor should be observed, which acts to partially bandlimit the input signal as well as lower slew-rate dependent distortion, even though the feedback factor remains close to unity of a broad frequency range.

3-2   Mild amplifier non-linearity

In Section 2-2-2 a transimpedance stage with mild non-linearity was analysed while operating with a sampled data time-domain waveform. Simulation results presented here are performed with the following characteristics selected to prevent the onset of slew-rate limiting even at the lowest sampling rate of 48 kHz:

Positive and negative slew rates: $S_+ = 500$ V/μs $S_- = -500$ V/μs

Transimpedance amplifier first break frequency: $f_0 = 100$ Hz

Signal resolution: 24 bit

Non-linearity parameters of operational amplifier: $\lambda_1 = 0.01$ $\lambda_2 = 0.001$ $\lambda_3 = 0.0001$

Input consists of two sinusoidal currents each of amplitude $\sqrt{2}$ mA and respective frequencies 19 kHz and 20 kHz, where the low-frequency transimpedance is 1 kΩ, where the assumed peak-to-peak current output range of the DAC is $-2\sqrt{2}$ to $2\sqrt{2}$ mA. Output spectra are shown in Figures 3-5a, 3-6a and 3-7a respectively for sampling rates of 48 kHz, 192 kHz and 384 kHz together with corresponding equivalent time-domain jitter waveforms shown in Figures 3-5b, 3-6b and 3-7b. Two sine wave reference signals are also superimposed on the spectra to benchmark the 24-bit dynamic range, one at set at the full amplitude of $2\sqrt{2}$ mA peak, while the other is reduced in level by 2^{24} (i.e 144 dB).
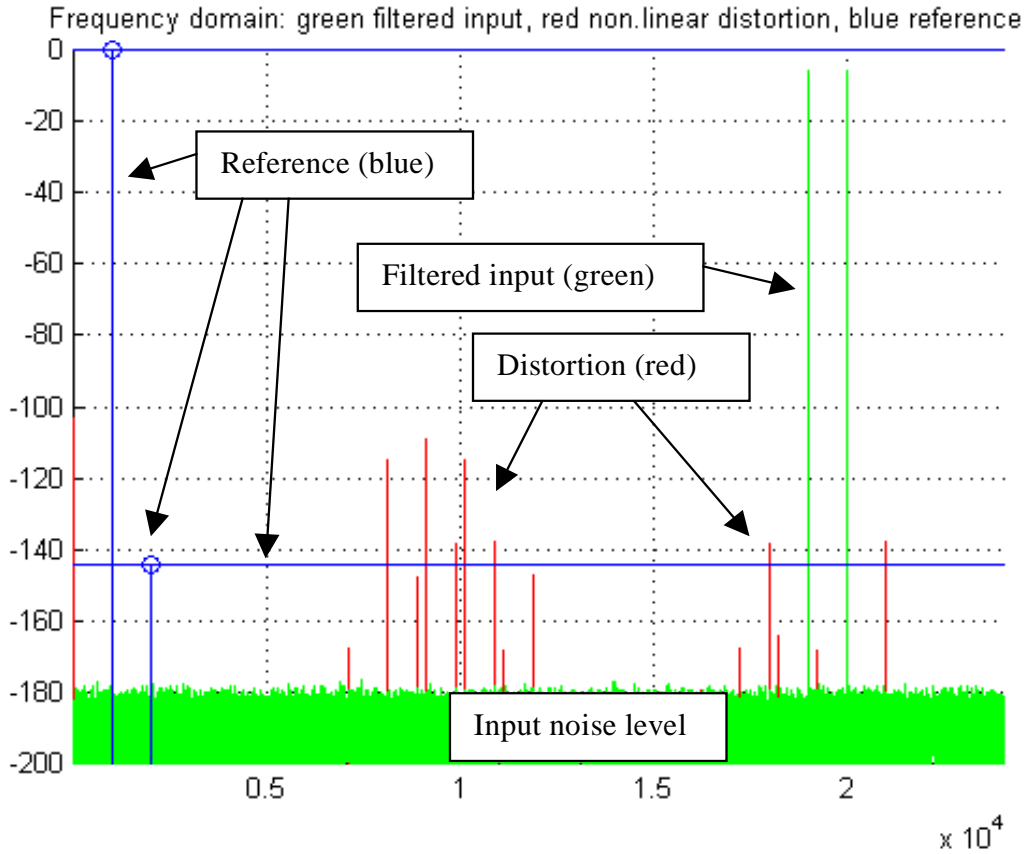
10

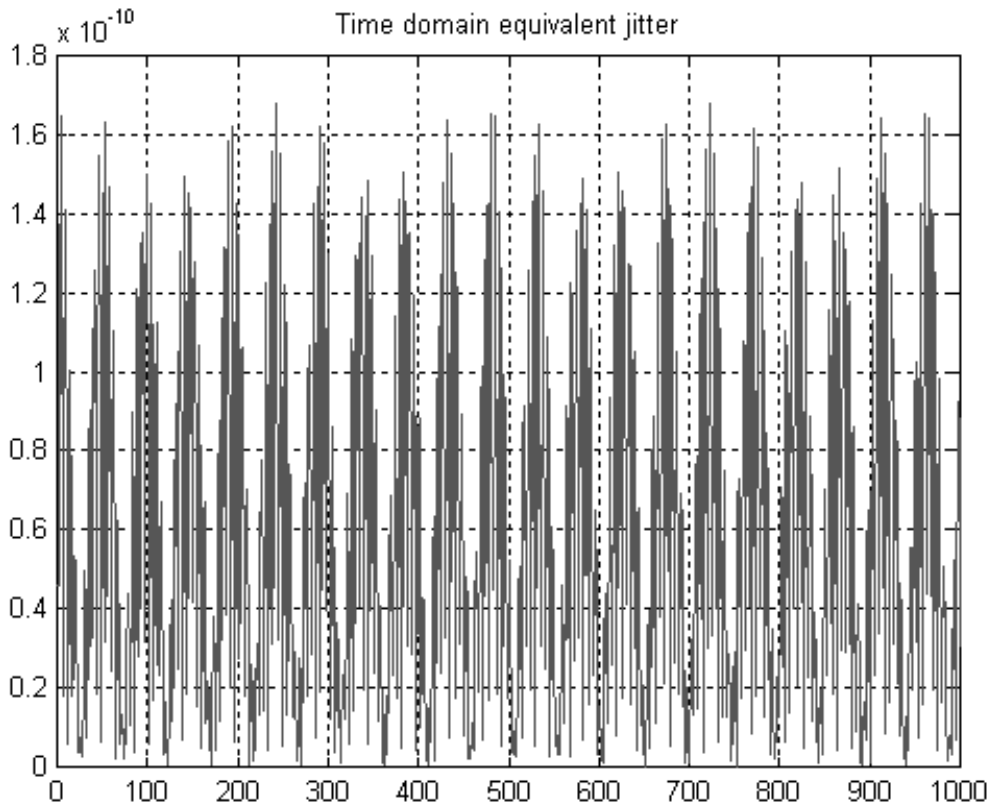**Figure 3-5a Output spectrum, sampling rate 48 kHz**

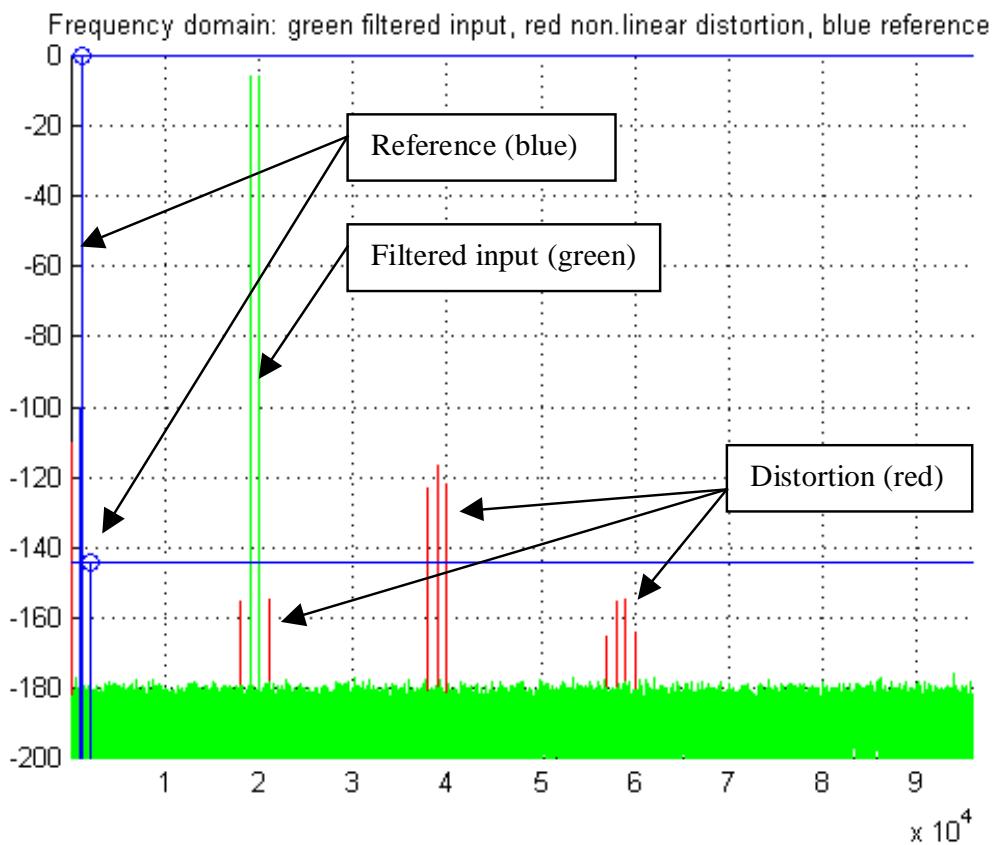**Figure 3-5b Equivalent sampling jitter, sampling rate 48 kHz.**

11

Frequency domain: green filtered input, red non.linear distortion, blue reference

Reference (blue)

Filtered input (green)

Distortion (red)

Figure 3-6a Output spectrum, sampling rate 192 kHz.

Time domain equivalent jitter
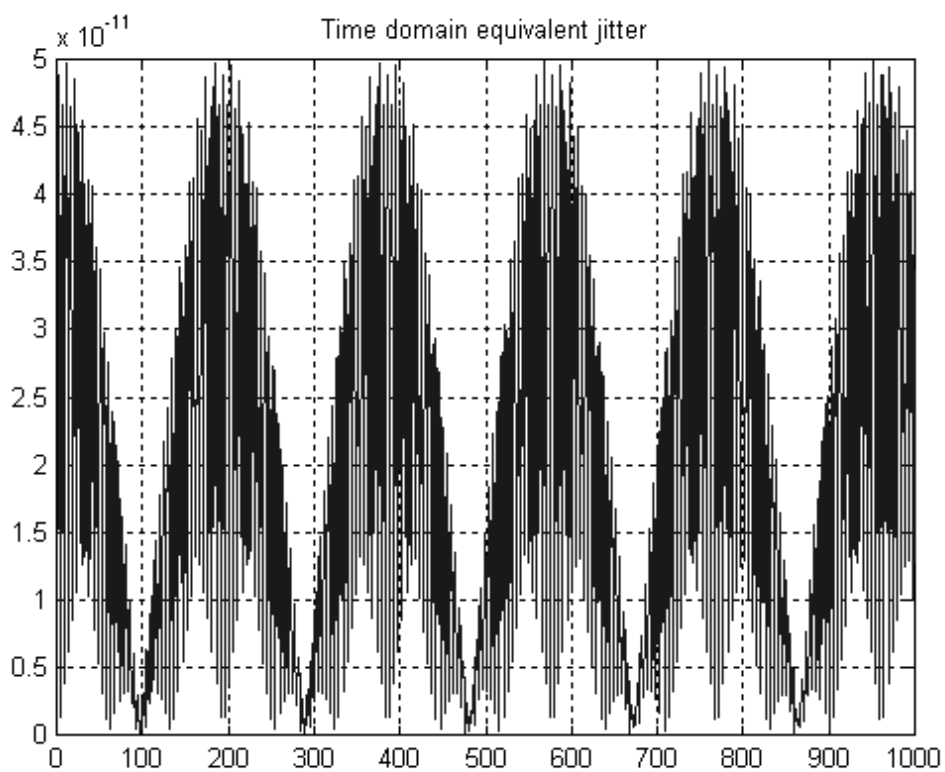
Figure 3-6b Equivalent sampling jitter, sampling rate 192 kHz.

12
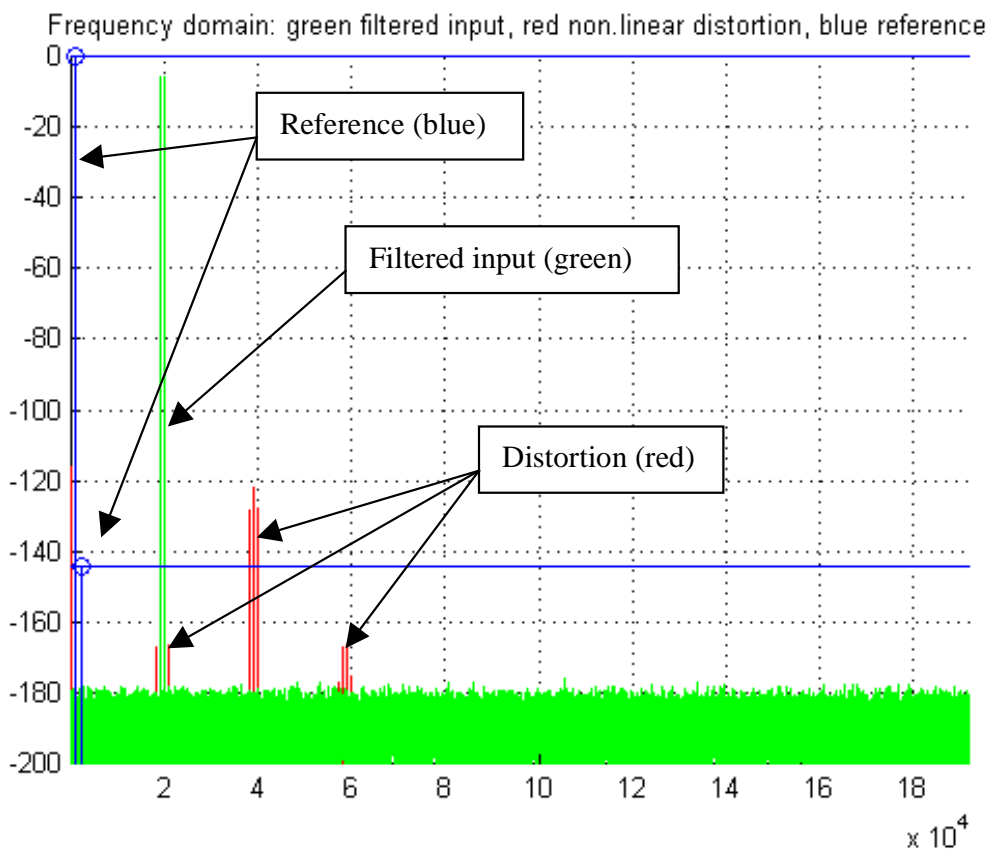
Figure 3-7a Output spectrum, sampling rate 384 kHz
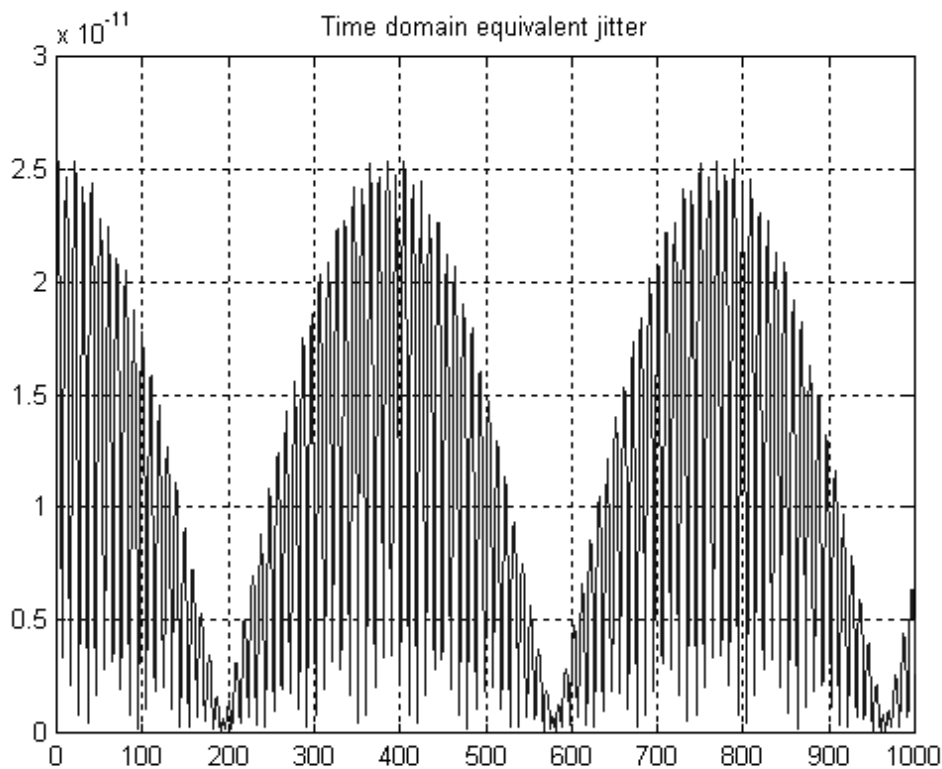
Figure 3-7b Equivalent sampling jitter, sampling rate 384 kHz.

13

3-3 Mild amplifier non-linearity with slew-rate limiting

In Section 2-2-3, the analysis was extended to include slew-rate limiting. As to whether slew-rate limiting occurs depends upon the inter-sample difference and the closed-loop bandwidth f_0 of the transimpedance stage. By way of example, the simulations presented in 3-2 are repeated but with the slew-rate limits of the operational amplifier modified to,

Positive and negative slew rates: $S_+ = 50$ V/μs $S_- = -50$ V/μs

Output spectra are shown in Figures 3-8a, 3-9a and 3-10a respectively for sampling rates of 48 kHz, 192 kHz and 384 kHz together with corresponding equivalent time-domain jitter waveforms shown in Figures 3-8b, 3-9b and 3-10b.

3-4 Observations

In the following discussion the objective is to compare distortion levels against a system aspiring to 24-bit resolution. As the sampling rate is lowered, inter-sample differences increase so increasing the differential drive to the transimpedance stage, hence higher distortion is anticipated. However, it is evident that the greatest distortion arises because of slew-rate limiting, even if this is only a momentary event at the commencement of each sample, so it is imperative to design a system such that amplifiers operates well clear of slope overload. Although the slew rate in the analysis was referred to the output voltage, it is conceivable that other slope related distortions could occur in the operational amplifier. This was partially accounted by the inclusion of a mild non-linearity operating on the inter-sample difference signal.

The use of equivalent jitter was used to demonstrate how distortion calculated on a sample-by-sample basis compares with conventional timing jitter, as notional benchmarks have been suggested as to permissible levels of jitter. For example, critical listening tests have been used to evaluate the effect of sampling rate on audible performance. Interestingly, results suggest that the level of jitter must be held to an extremely low level for valid results to be obtained.   Of course this is an oversimplification, as the spectral content of jitter and its correlation with the signal are critical and the interactions can be extremely complicated. It is evident that quite mild levels of non-linearity in the open-loop behaviour of an operational amplifier can map through to equivalent jitter figures that are significant. The linear analysis presented in Section 3-1 is illuminating with regard to this phenomena, where dynamic modulation of the parameters such as dc gain and/or the dominant-pole frequency, will map effectively into timing errors. It is important to note that parametric modulation is exacerbated by the presence of rapid signal changes at the sample boundaries, where one can envisage a transient modulation of pulse timing, making the concept of jitter equivalence more tractable. However, if the signal is filtered to remove the sample structure this should reduce the level of modulation, where this appears to be born out by the process of pre-filtering of the DAC output current prior to I/V conversion.

The inclusion of capacitor C_f in the feedback path reduces the output slew-rate. Consequently, in this sense is helpful but because the DAC output impedance is high, the capacitor has little effect on the level of feedback which is already close to maximum, so will not influence the output distortion other than by introducing high-frequency attenuation of the input. Inter-modulation and timing modulation remain. Observe how in the analysis in Section 2-2-1, group delay changes with operational amplifier dc gain A_{v0} occurred even when capacitor C_f was included in the feedback loop. Although C_f has no direct effect on timing performance, it does affect distortion resulting from rapid output voltage changes, which in turn then modulates the amplifier parameters, hence dynamically altering in-band group delay.

To mitigate the problem of timing modulation three strategies are proposed:

- Open-loop/current-feedback, wide-band I/V conversion where the in-audio band, signal delay is low and the amplifier parameters are established with minimal parametric modulation.
- Pre-filter the DAC output current with a passive low-pass filter.
- Multiple amplifier stages with nested feedback to achieve extremely high loop gains with low in-band phase group delay distortion.

Section 4 discusses low-feedback current-steering circuits, while pre-filtering is investigated in Section 5 and a dual-loop I/V stage is presented in Section 6.
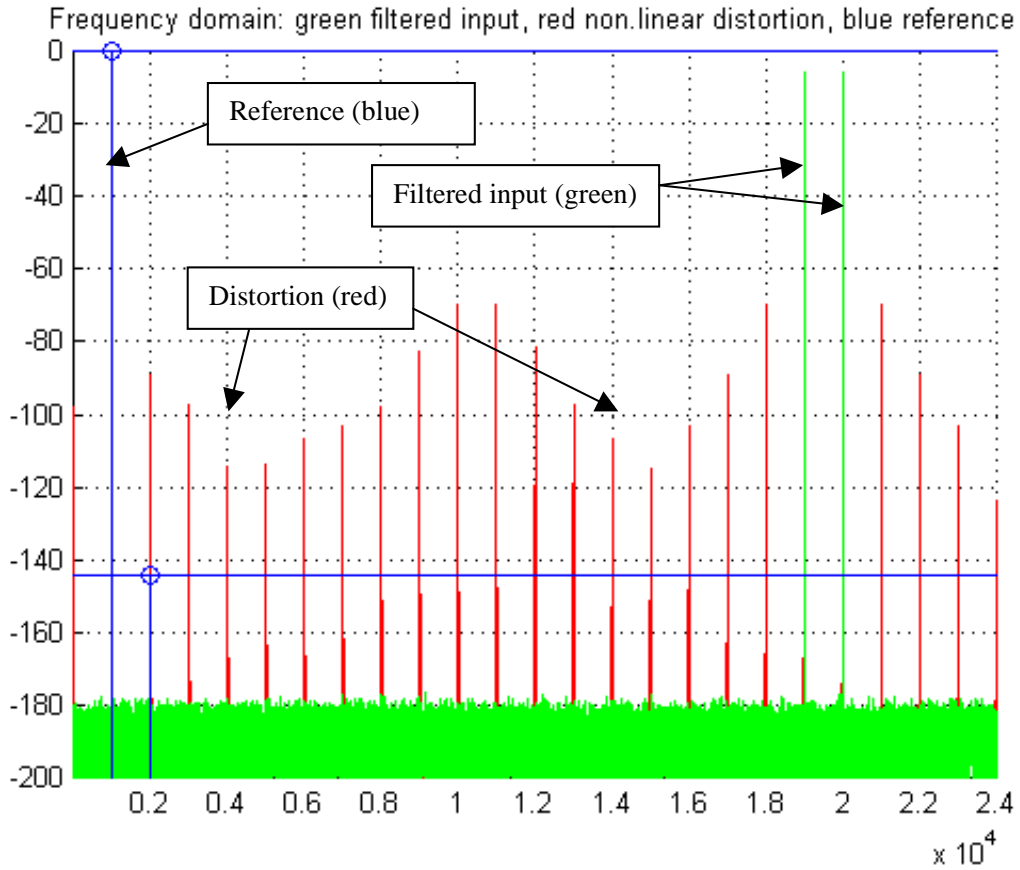
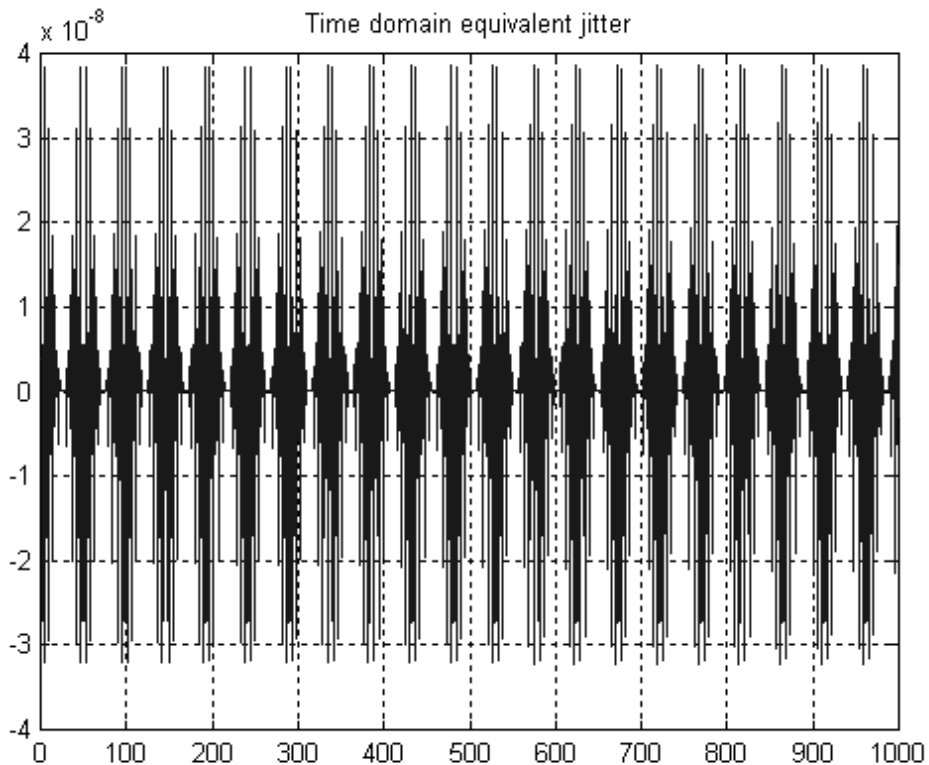**Figure 3-8a Output spectrum, sampling rate 48 kHz**

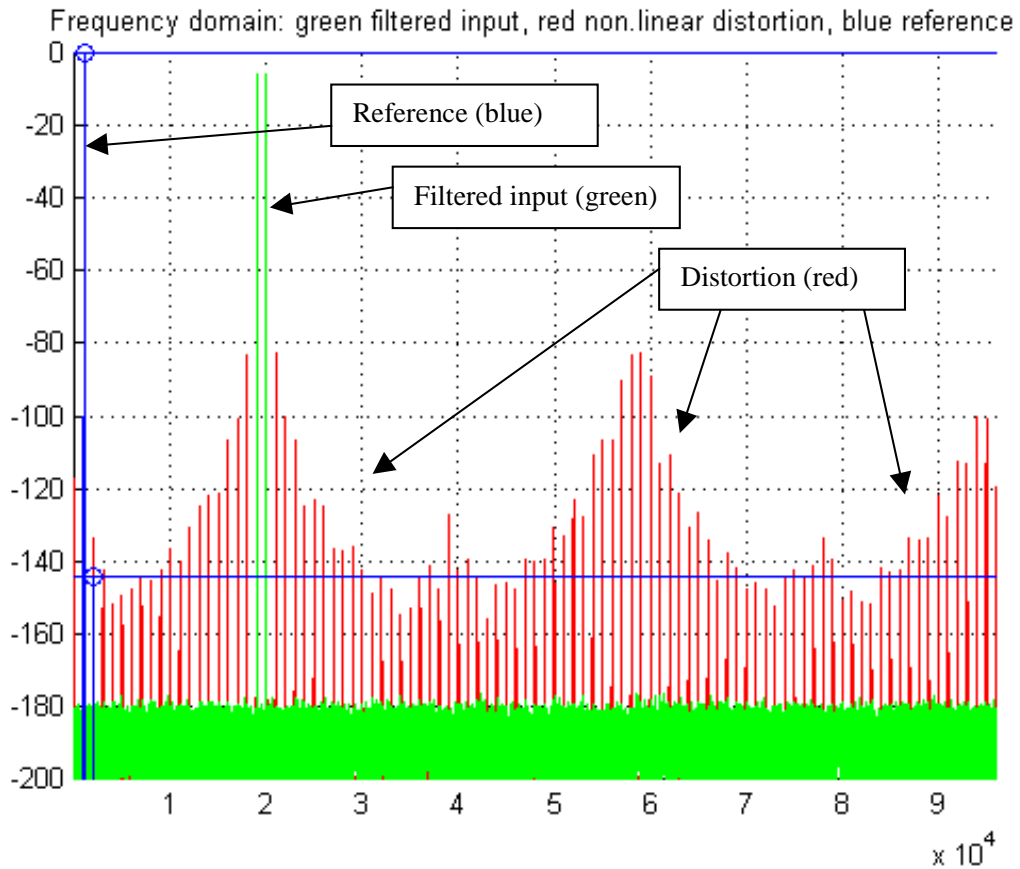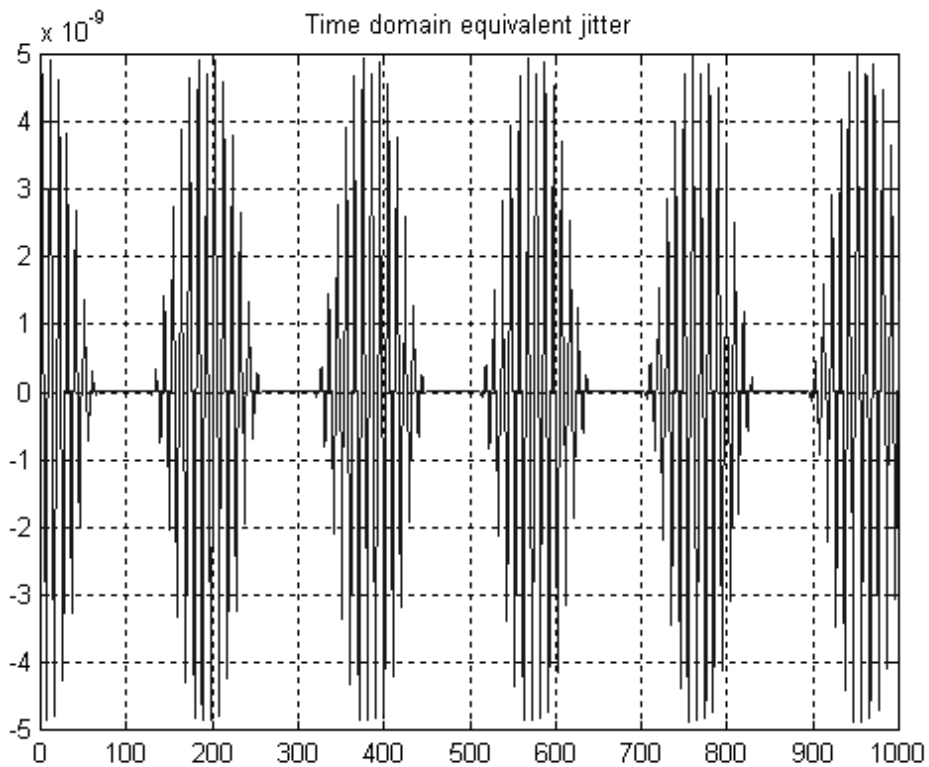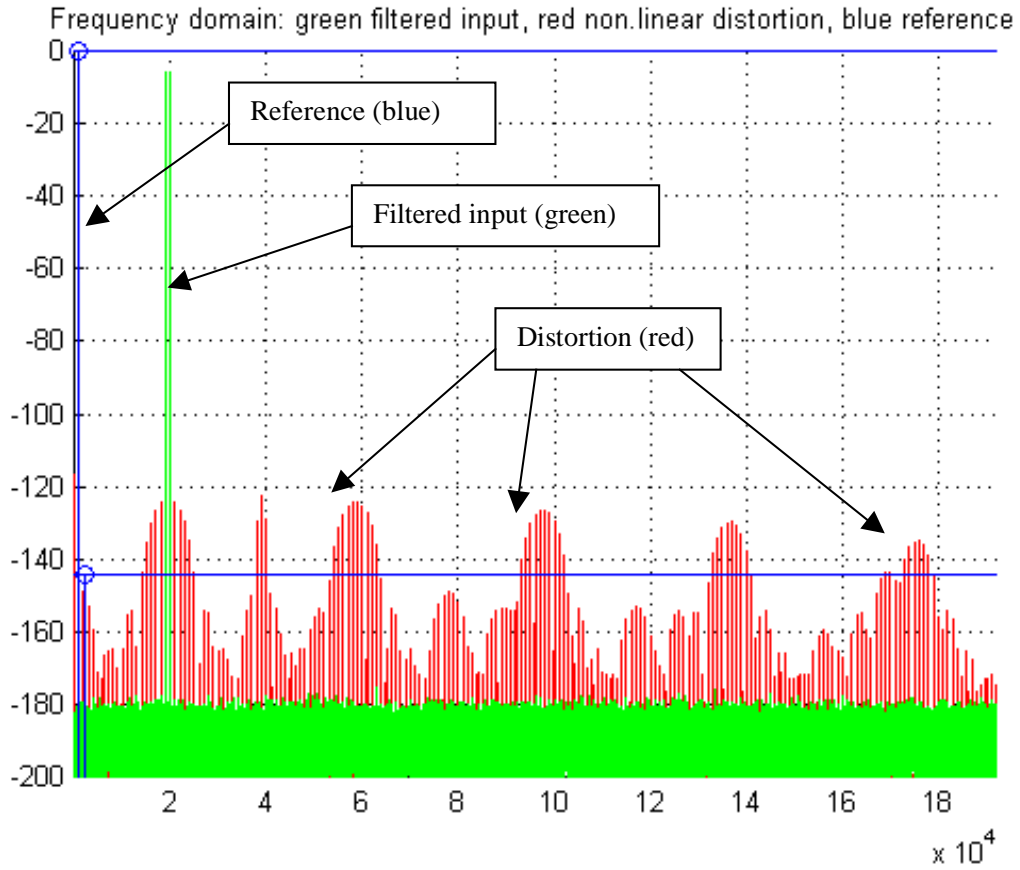**Figure 3-8b Equivalent sampling jitter, sampling rate 48 kHz.**

15

Frequency domain: green filtered input, red non.linear distortion, blue reference

Reference (blue)

Filtered input (green)

Distortion (red)

Figure 3-9a Output spectrum, sampling rate 192 kHz

Time domain equivalent jitter

Figure 3-9b Equivalent sampling jitter, sampling rate 192 kHz.

16

Figure 3-10a Output spectrum, sampling rate 384 kHz
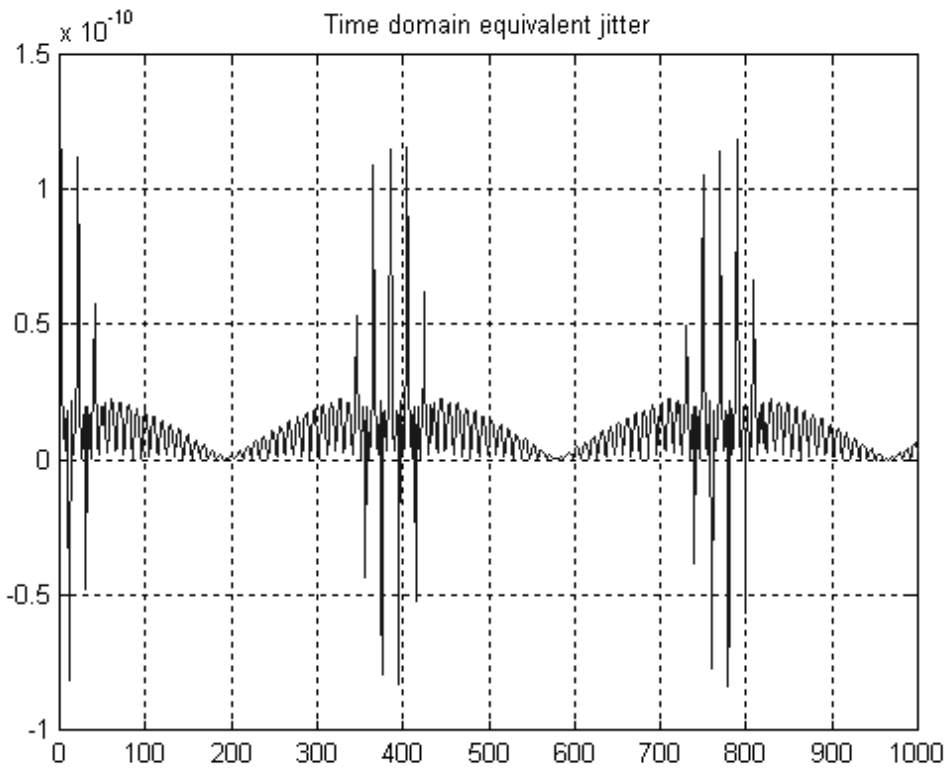
Figure 3-10b Equivalent sampling jitter, sampling rate 384 kHz.

17

4 Current-steering amplifiers

An alternative approach to the feedback amplifier is to use a current-steering, open loop configuration as shown conceptually and without dc biasing in Figure 4-1. This transimpedance stage uses a grounded-base amplifier that steers the output current of the DAC into the collector load impedance. The load impedance includes a shunt capacitance to partially bandlimit the signal and to reduce the rate of change of output voltage. For the special case of a DAC with infinite output impedance, the only distortion mechanism is the minor modulation in the slope parameters of the transistors. However, a finite DAC output impedance will result in minor distortion due to the modulation of input resistance with signal current. The amplifier is completed by using a unity-gain buffer amplifier and low-pass filter.
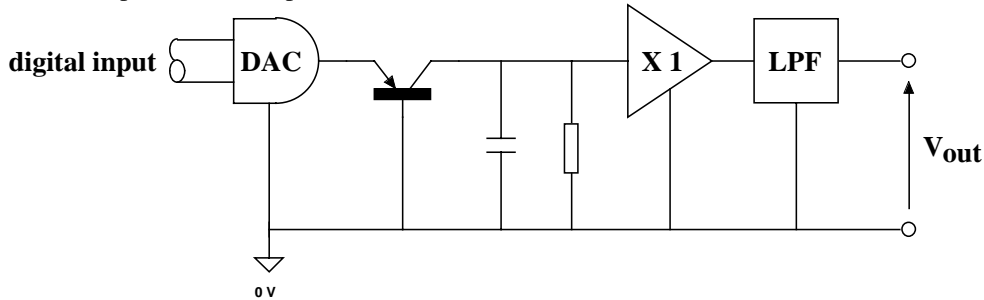

Figure 4-1 Grounded-base open-loop current steering transimpedance stage.

4-1 Input stage error correction

The use of optimally balanced, error feedback can virtually eliminate the non-linear modulation of transistor base-emitter slope resistance. In Figure 4-2 a modified amplifier is shown where the input stage consists of two matched complementary transistors T_1 and T_2 together with a grounded base stage T_3. T_1 and T_3 act as a cascode stage to steer the DAC output current i to the current mirror formed by T_4, T_5 and the three equal valued resistors R_0 such that the collector currents of T_4 and T_5 each carry a mirror the current i. As a result, changes in emitter currents of T_1 and T_2 are identical, where providing parametric and thermal matching, then $V_{BE1} = -V_{BE2}$. Consequently, the emitter potential of T_1 remains theoretically zero even though the base-emitter voltages may change non-linearly with signal current. This implies zero input impedance even under large signal conditions. A constant current generator I_B sinks the collector current bias component of T_5 while a parallel resistor-capacitor network R_1, C_1 converts the DAC signal current to a voltage. A unity-gain buffer with high input impedance completes the conversion yielding an overall transimpedance $Z_{I/V}$ of,

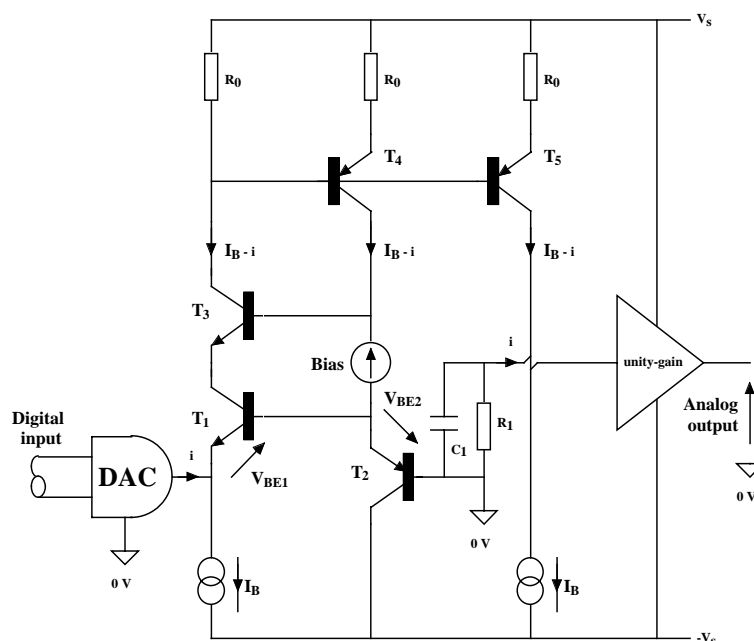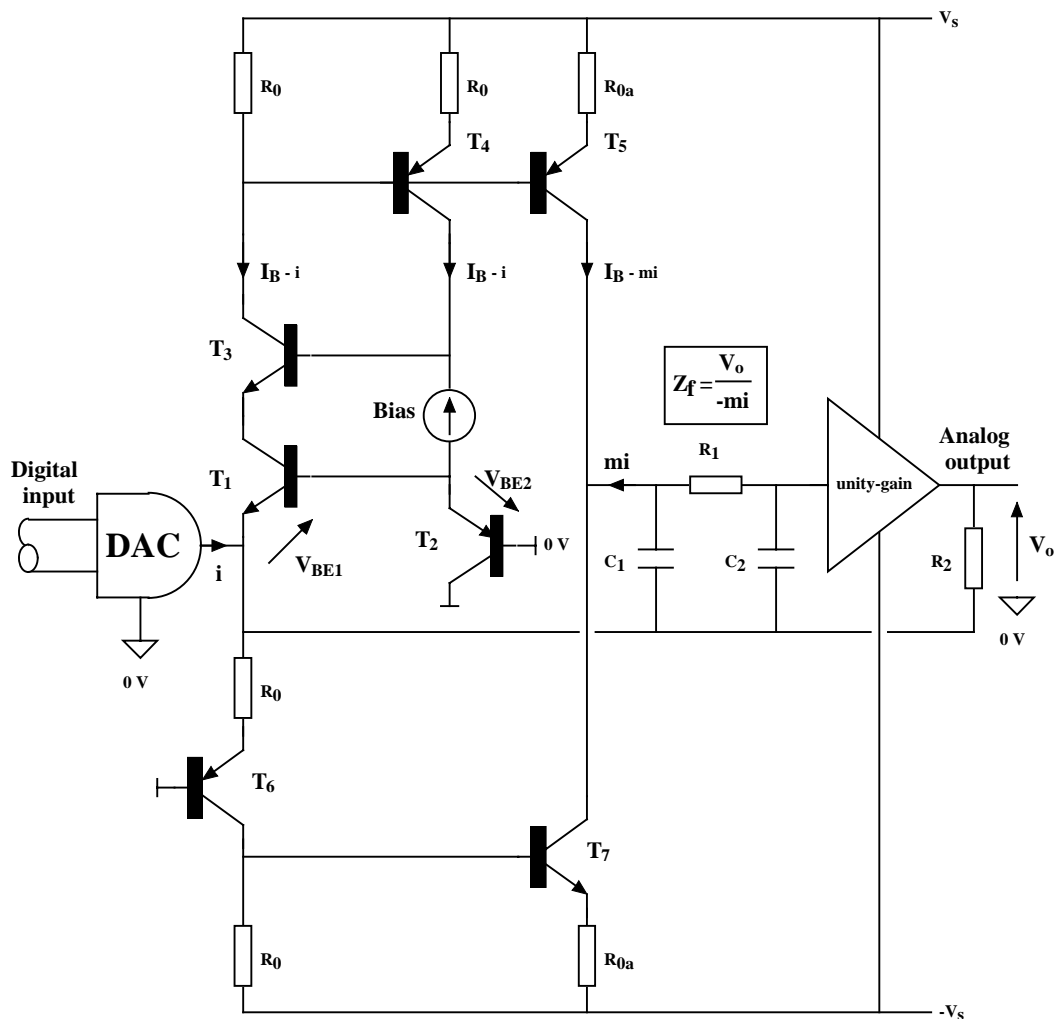$$Z_{I/V} = \frac{-R_1}{1 + j\omega R_1 C_1} \qquad \dots 4\text{-}1$$

Figure 4-2 Open-loop transimpedance amplifier with input stage error correction.

4-2   Current-feedback transimpedance amplifier, embedded low-pass filter

The performance of the transimpedance amplifier can be improved by current feedback as shown in Figure 4-3.

Figure 4-3 Transimpedance amplifier with error correction and embedded low-pass filter.

A principal feature of this circuit is the inclusion of a second-order, low-pass filter embedded in the output stage formed by the π-network R_1, C_1 and C_2, a unity-gain buffer and resistor R_2. However, it will be observed that the filter ground line is returned to the input node rather than the true ground and this constitutes the current-feedback path to the emitter of T_1. The operation is such that at low frequency, feedback is derived via R_2 and thus includes the output buffer, while at higher frequency, in the filter attenuation region, the current path is derived primarily from the collector current of T_6.

In this respect the high-frequency feedback path is similar to a simple dc-coupled feedback pair of transistors. Benefits derived from this configuration include reduced output impedance and enhanced linearity together with an embedded low-order reconstruction filter, where the filter behaves as an integral part of the feedback path while returning no currents to ground to aid ground-rail purity. Although a second-order low-pass filter is shown in Figure 4-3, higher-order filters can be accommodated without incurring a stability penalty. In effect, the low-pass filter acts as a nodal transition filter, allowing the feedback path to be gradually redirected as a function of frequency from the output node to the buffer input. Also, the DAC signal current i is returned to the power supply and does not require transient currents to flow in the ground bus.

Assuming the current gain of the mirror formed by transistors T_4 and T_5 is m and the filter formed by C_1, R_1 and C_2 has a transimpedance Z_f (see Figure 4-3 for component definitions), then the closed-loop transimpedance $Z_{I/V}$ of the overall amplifier is,

$$Z_{I/V} = \frac{-R_2}{1 + \left(\frac{1+m}{m}\right)\dfrac{R_2}{Z_f}} = \frac{-R_2}{1 + \alpha\dfrac{R_2}{Z_f}} \qquad \ldots \text{4-2}$$

where $\alpha = m/(m+1)$. Taking the filter example shown in Figure 4-3, then the transimpedance of this filter stage Z_f is,

$$Z_f = \frac{1}{j\omega(C_1 + C_2) + (j\omega)^2 R_1 C_1 C_2} \qquad \ldots \text{4-3}$$

resulting in,

$$Z_{I/V} = \frac{-R_2}{1 + j\omega\alpha R_2(C_1 + C_2) + (j\omega)^2 \alpha R_1 C_1 R_2 C_2} \qquad \ldots \text{4-4}$$

4-3   Discrete transimpedance amplifier with input-stage error correction

Figure 4-4 illustrates a complete transimpedance amplifier based upon the skeleton topology presented in Section 4-2. This circuit incorporates a second-order, low-pass output filter together with an optional RC network to implement the standard de-emphasis characteristic required for CD replay. A servo amplifier is also included to control the output voltage offset voltage to facilitate dc coupling. The overall transimpedance of this amplifier without de-emphasis but including a first-order servo follows as,

$$Z_{I/V} = \left[\frac{-1100}{1 + j\omega 11*10^{-6} + (j\omega)^2 2.42*10^{-12}}\right]\left[\frac{j\omega*10}{1 + j\omega*10}\right] \qquad \ldots \text{4-5}$$
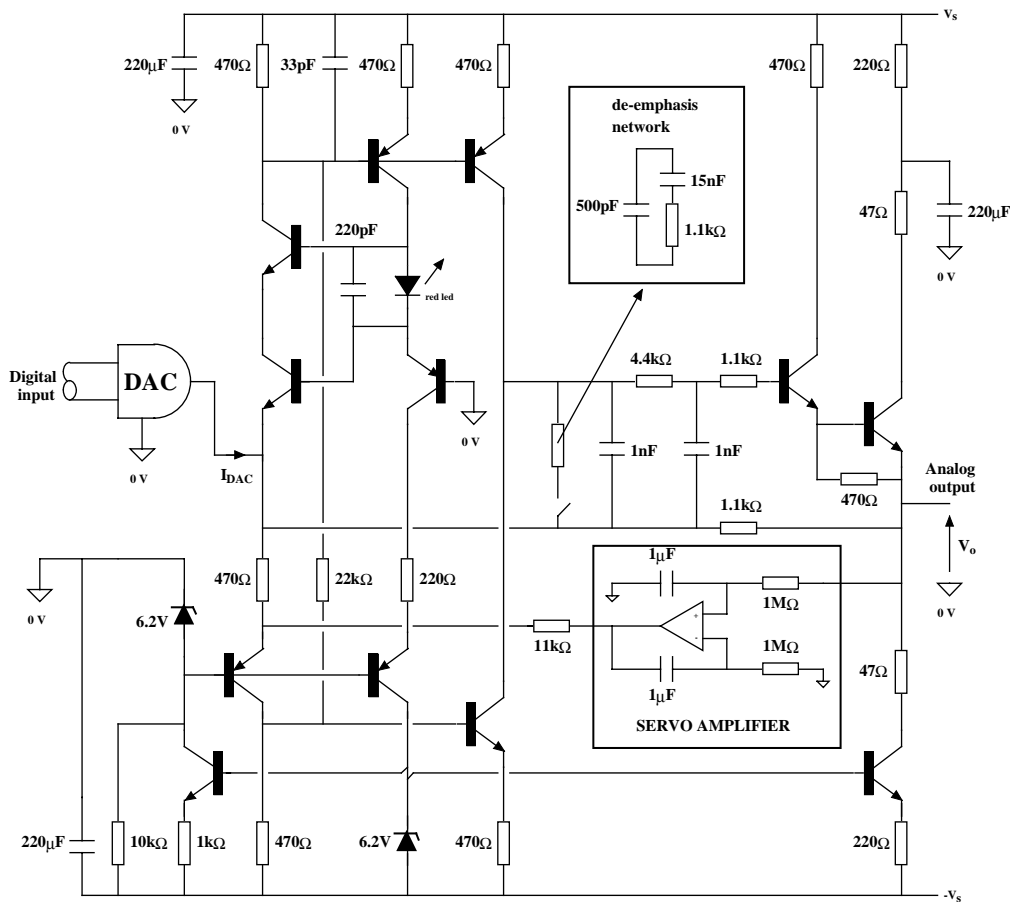

Figure 4-4 I/V stage with error correction, embedded low-pass filter and servo amplifier.

5 DAC output current pre-filter prior to I/V conversion

To reduce the rate-of-change of signal current applied to the transimpedance stage, pre-filtering can be used where an example circuit is shown in Figure 5-1.
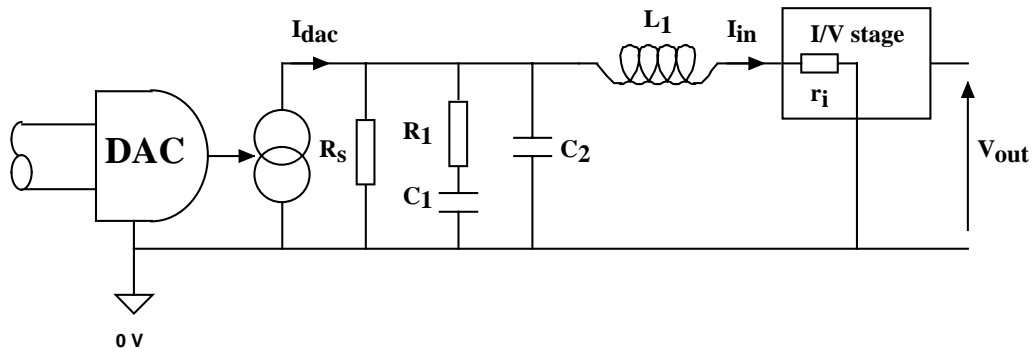

Figure 5-1 Pre-filter for DAC output current using lumped RLC network.

The filter band-limits the input current prior to conversion and militates against distortion resulting from rapid signal changes occurring at sample boundaries, thus lowering distortion correlation with the sampling rate. However, a negative feature of this technique is that it reduces the source impedance seen by the transimpedance stage, which has a detrimental effect on distortion and noise performance. Also, the input impedance of the filter changes with frequency implying that the DAC no longer feeds a near zero impedance. Nevertheless, such additional processing is often effective in association with low-cost operational amplifier transimpedance stages.

6 Dual-loop transimpedance stages

An enhancement to the single operational amplifier I/V stage is shown in Figure 6-1, where three operational amplifiers are used together with nested-differentiation feedback to achieve stability [7,8,9].
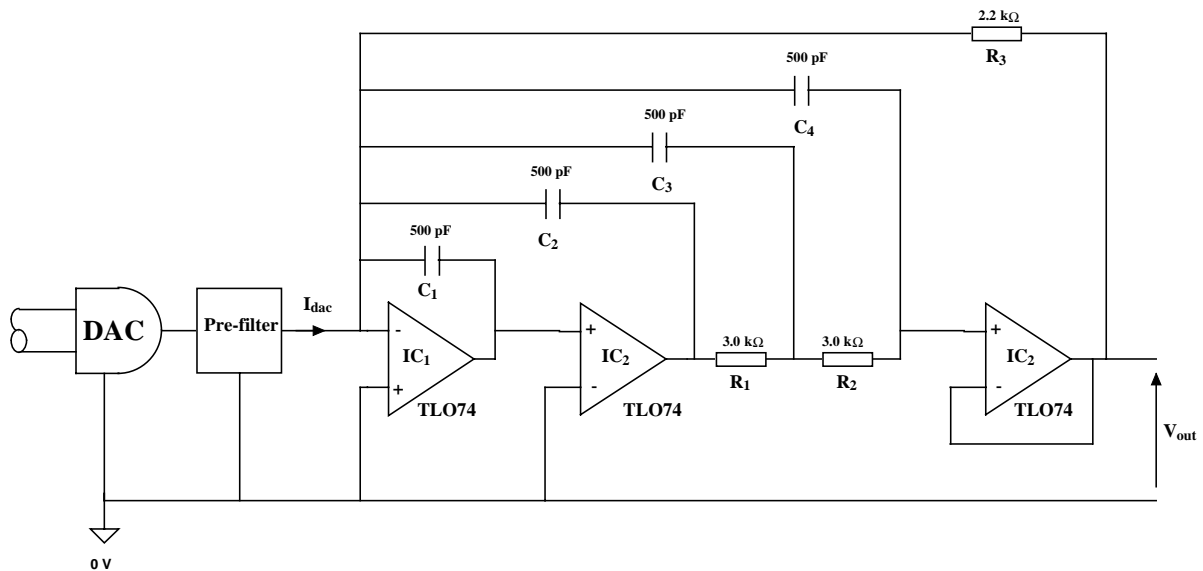

Figure 6-1 Dual-loop operational amplifier transimpedance stage with nested-differentiating feedback configured as a 3rd-order low-pass filter.

Two operational amplifiers are used for amplification, while the third is used as unity-gain output buffer. Nested feedback has a dual function and also forms a third-order, low-pass filter for signal recovery. The principal advantage of dual stages is a large reduction in sensitivity to the operational amplifier characteristics that achieves a corresponding reduction in dynamic phase modulation. Amplitude and phase responses are shown in Figure 6-2 for a design configured for a 50 kHz signal bandwidth, where the input reference current level is 1 mA. Figure 6-2 also shows the output response of the first operational amplifier IC_1, where the signal level is typically better than 70 dB below that of the final output, this helps to reduce transient modulation in IC_1 by constraining its output signal amplitude.

21
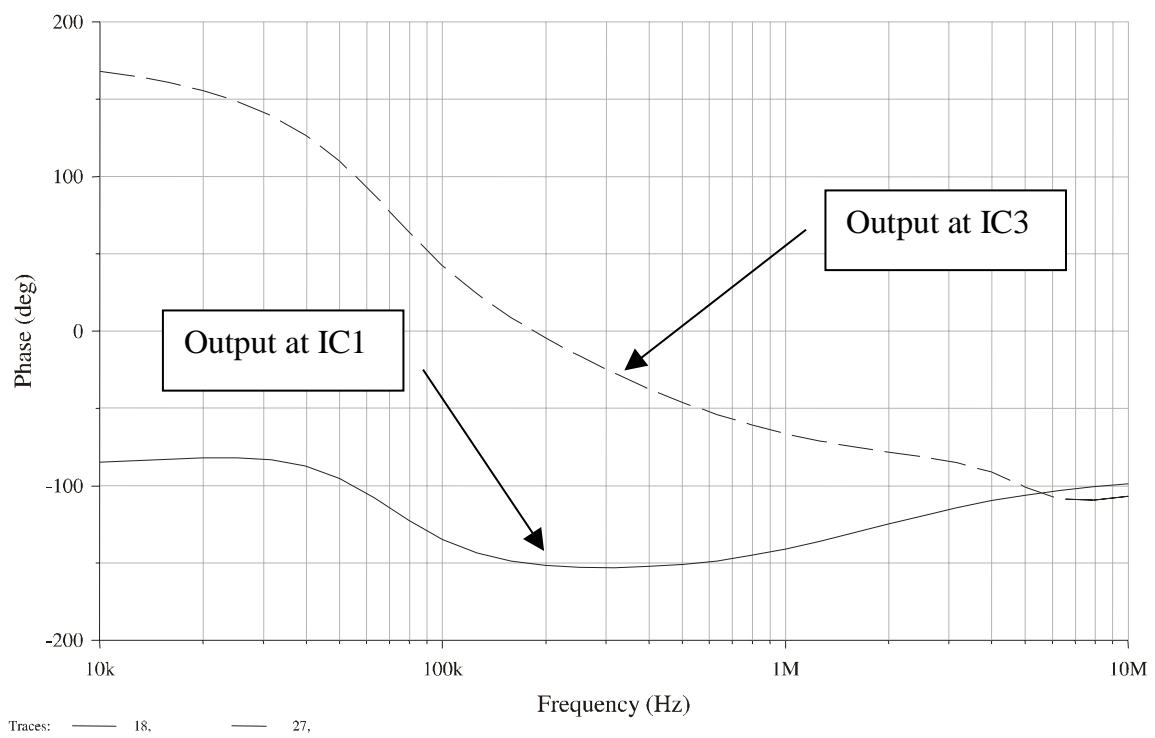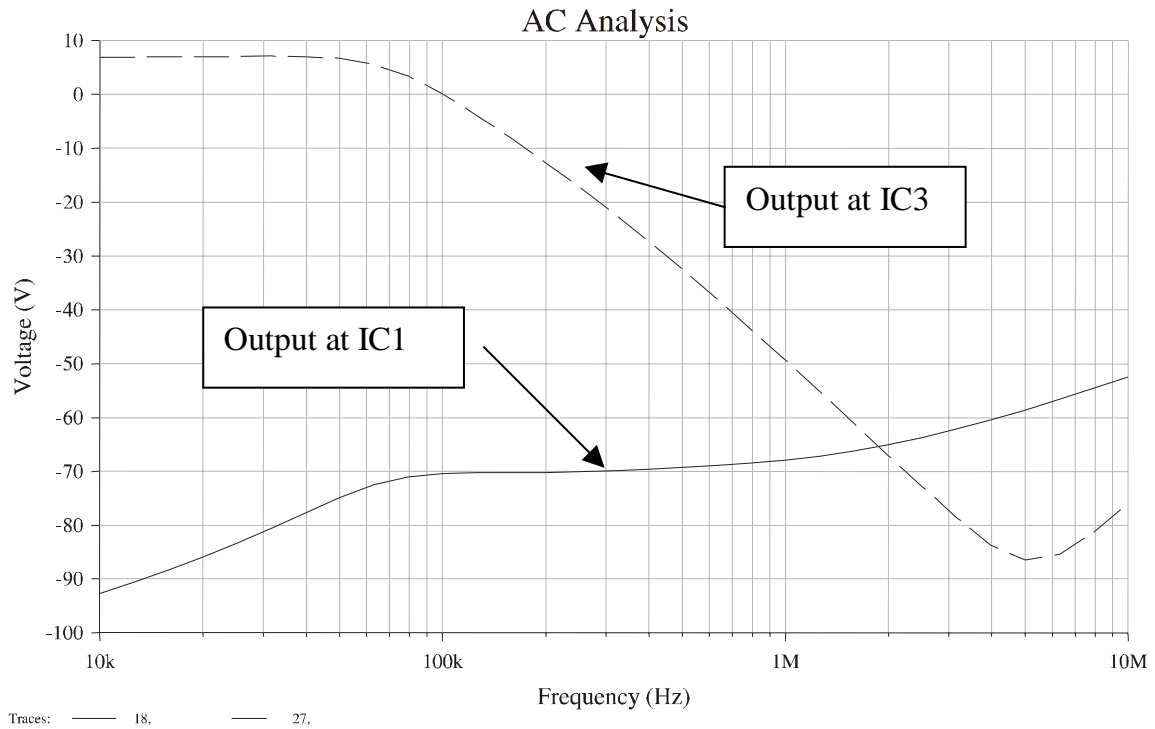
**Figure 6-2 Transimpedance amplitude and phase response plots (reference Figure 6-1).**

Next, some aspects of overall error of a 2-stage I/V stage are investigated. Figure 6-3 shows a pair of 2-stage transimpedance amplifiers with an error signal derived from the difference of their respective outputs, where this configuration is used as a simulation model. By way of example and to demonstrate the sensitivity of the overall error to operational amplifier gain, the input current to output error voltage response is shown in Figure 6-4 for a first-stage gain error g = 0.9. Because two stages of amplification are used, it follows that the low-frequency error has only a small phase shift of less than 20 degree. This coupled with a low level of error < -175 dB, means that the overall transimpedance has extremely low sensitivity to gain changes. By way of comparison, if the second stage is removed, Figure 6-5 shows the corresponding error level which is now only a little below –97 dB with a corresponding error signal phase shift of about -90 degree.

The observation that for the two-stage amplifier the error signal is almost in-phase is advantageous when considering equivalent jitter-distortion as a modulation in loop gain does not produce the same degree of differential-phase distortion as when the error is approximately in phase quadrature. Of course, the sensitivity being so much lower than for a single stage amplifier should virtually eliminate this problem and make the stage perform much closer to the specification dictated by high-resolution audio.
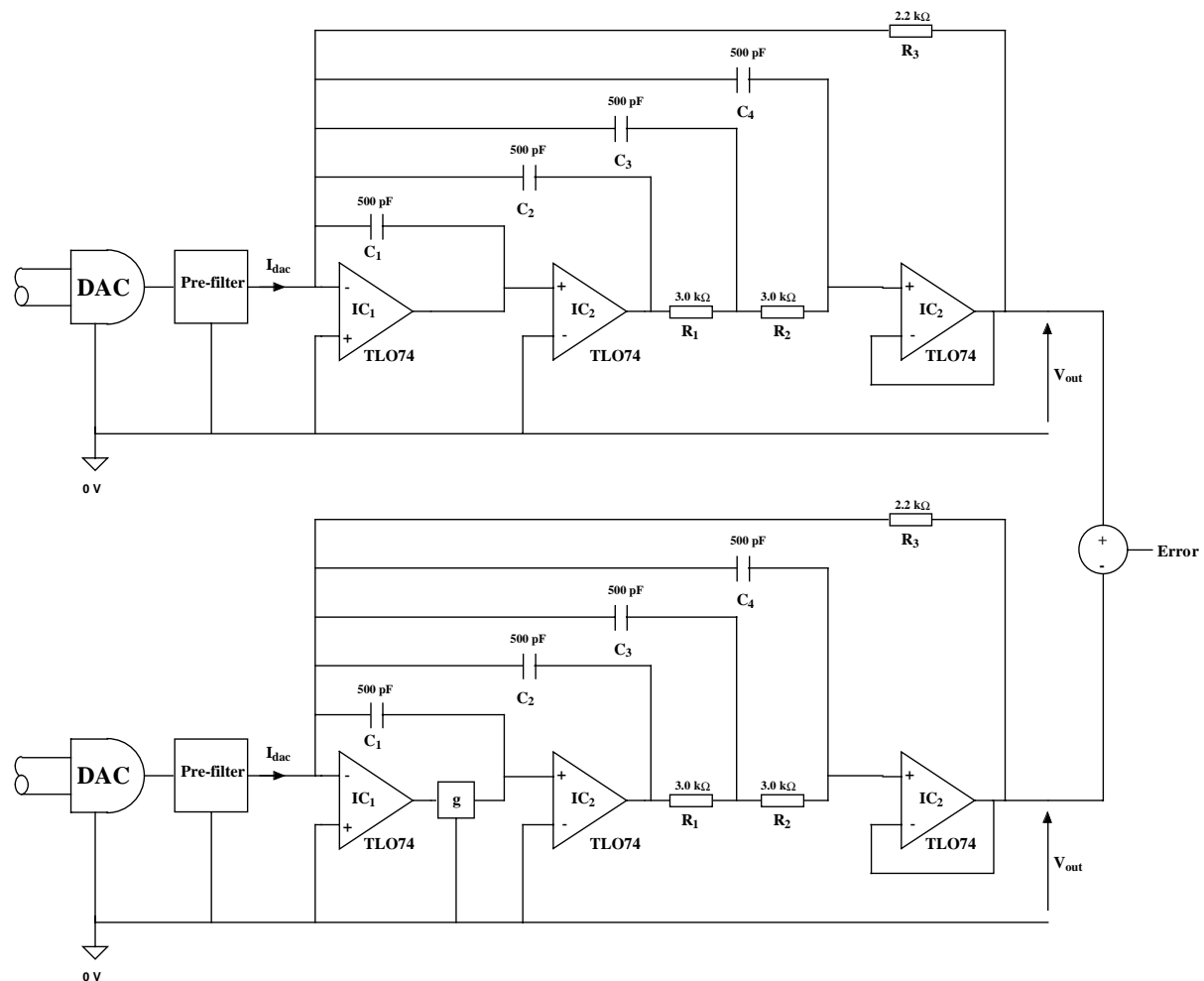
Figure 6-3 Parallel amplifier structure for determining error signal due to loop-gain error g.

23

2-stage_I-V_5

AC Analysis

Amplitude response of error signal (dB-frequency)
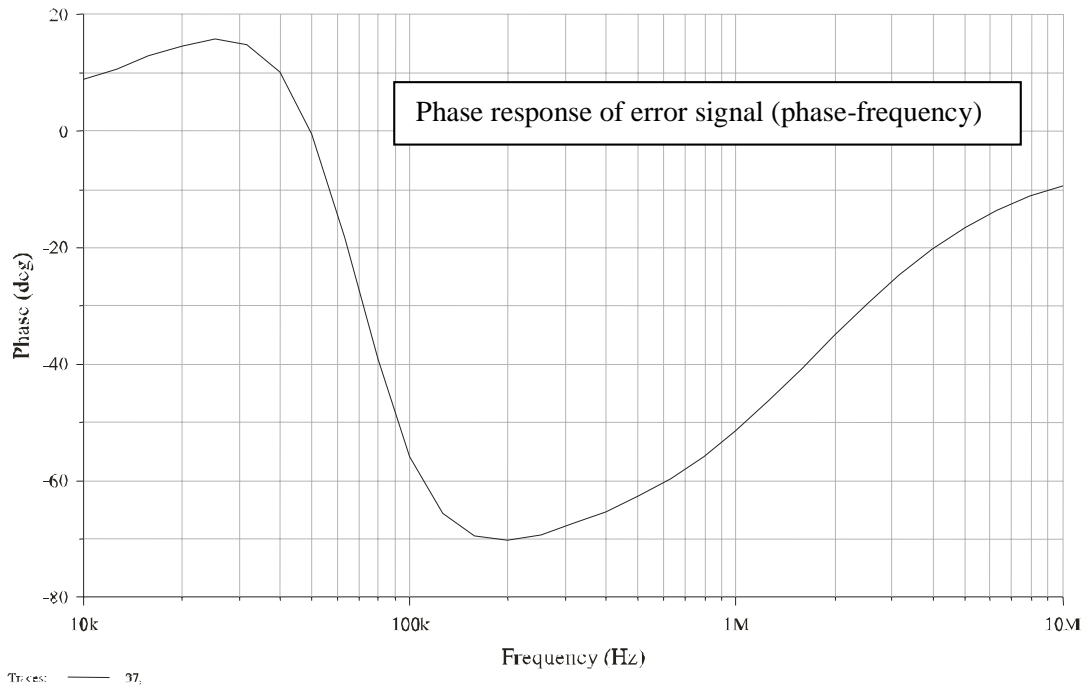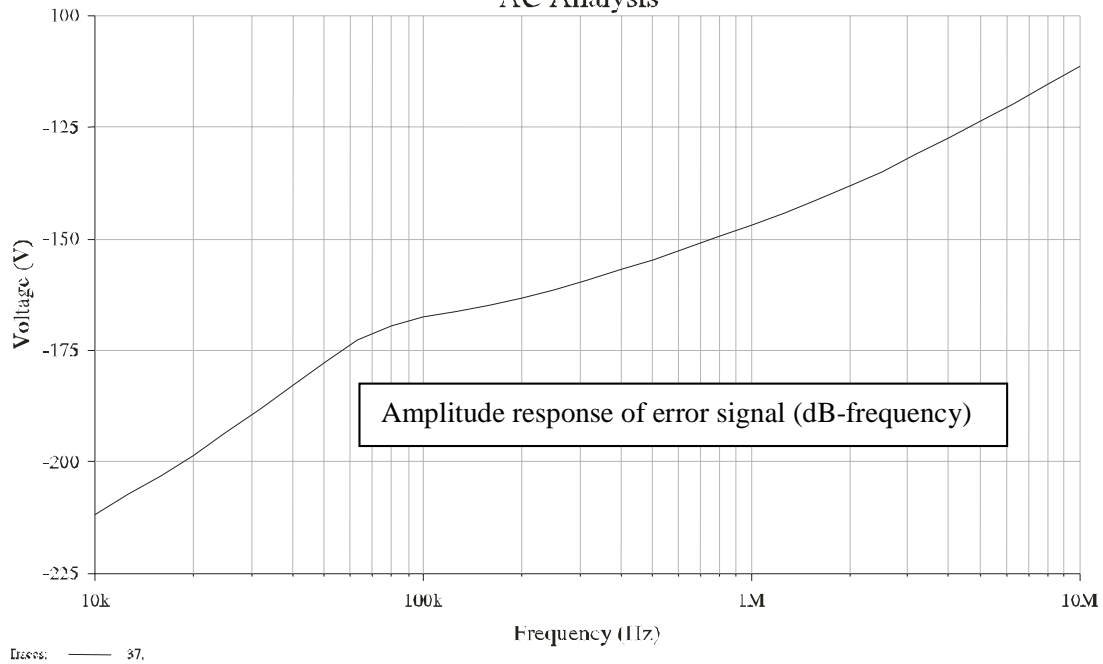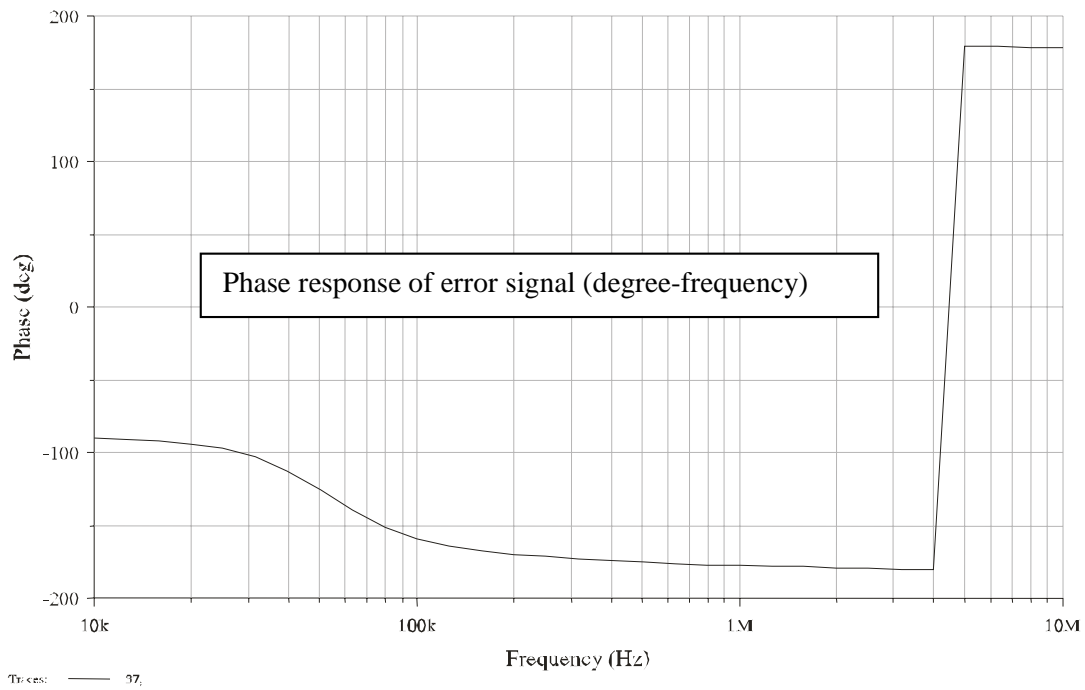
Phase response of error signal (phase-frequency)

Figure 6-4 Error signal for 2-stage amplifier with 0.9 gain error in first stage.

AC Analysis

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Amplitude response of error signal (dB–frequency)

Traces: ———— 37,

Phase response of error signal (degree-frequency)

Traces: ———— 37,
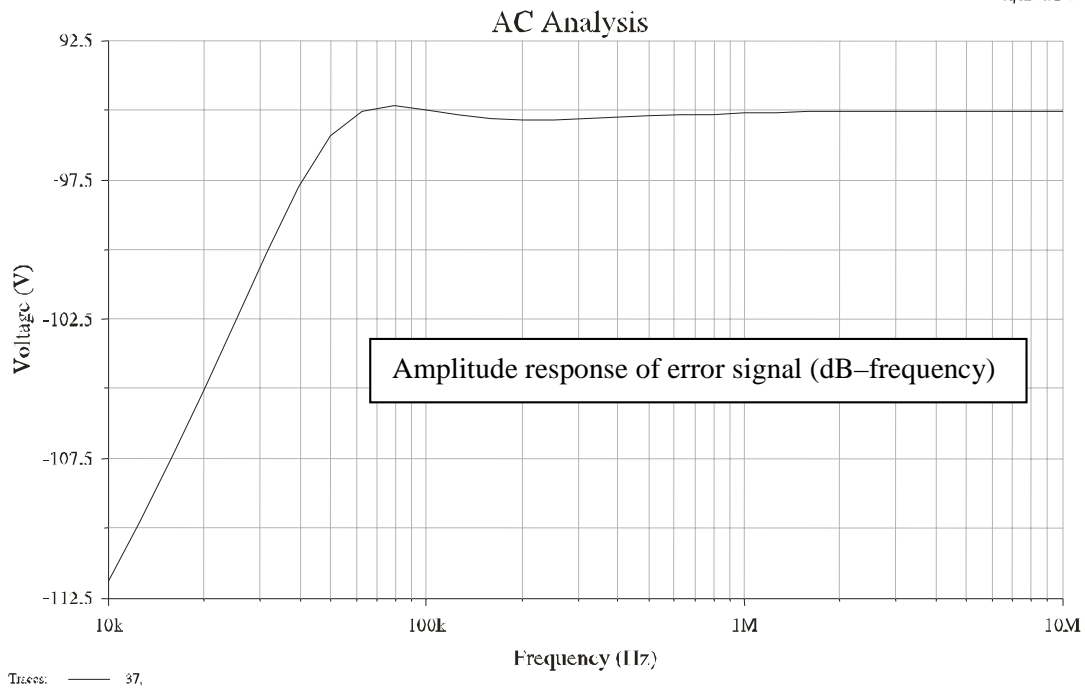
Figure 6-5 Error signal for 1-stage amplifier with a gain error of 0.9.

7   Conclusion

The design of current-to-voltage converters for high-resolution audio systems has been shown to be critical especially as transresistance amplifier non-linearity can be induced by the high-frequency signal components present in sampled audio signals at the output of a DAC. A number of distortion mechanisms have been discussed and the concept of jitter equivalence emphasised. Jitter is a performance indicator widely understood in digital audio, consequently transforming the distortion generated in an I/V conversion stage into an equivalent jitter sequence that is superimposed onto the sampled audio signal, forms a useful benchmark as well as unifying some aspects of the distortion.

As well as a detailed investigation of distortion mechanisms, the paper presented a number of circuit-level solutions using both discrete and operational amplifier topologies. Also, the use of input-stage error correction was illustrated. A method was described that enabled the low-pass recovery filter to be embedded into the topology where it became an integral structure within a nested-differential feedback topology. Such a technique allows the loop gain to be increased substantially, while band-limiting the signal within the transimpedance stage lowers slew-rate dependent distortion.

A dual-stage operational transimpedance amplifier was investigated and was shown to have a significantly lower sensitivity to operational amplifier loop-gain. It was also observed that the overall error signal in such stages has a significantly reduced phase shift at low frequency that is closer to 0 degree than to 90 degree, as occurs with a single stage amplifier. Another desirable attribute of the two-stage amplifier is that the output voltage of the first stage is extremely small, so eliminating slew-rate problems, while the embedded low-pass filter band-limits the signal applied to the second stage.

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